IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

RENESAS TECHNOLOGY CORP., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., -and- SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Civil Action No. _____ **JURY TRIAL DEMANDED**

COMPLAINT AND DEMAND FOR A JURY TRIAL

Nature of the Action

1. This is an action arising under the patent laws of the United States, Title 35, United States Code, for the willful infringement of United States patents.

The Parties

2. Plaintiff Renesas Technology Corp. ("Renesas or "Plaintiff"") is incorporated under the laws of Japan with its principal place of business at Marunouchi Building, 4-1 Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-6334.

3. Upon information and belief, defendant Samsung Electronics Co. Ltd. ("SEC") is a company incorporated under the laws of Korea with its principal place of business in Seoul, Korea. Upon information and belief, defendant Samsung Electronics America, Inc. ("SEA") is a New York corporation with its principal place of business in Ridgefield, New Jersey. Upon information and belief, SEA is a wholly-owned subsidiary of SEC.

Jurisdiction and Venue

4. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331, 1338(a).

5. This Court has personal jurisdiction under Del. Code Ann. Tit. 10, § 3104(c) on the basis that, upon information and belief, defendants SEC and SEA (collectively "Defendants") regularly have sold, directly or indirectly, and continue to sell infringing SDRAM products, or products containing same, to customers in Delaware, and Defendants derived and continue to derive substantial revenue therefrom.

6. Venue is proper in this District pursuant to 28 U.S.C. §§ 1391(b), (c) and 1400(b).

The Patents in Suit

7. On October 3, 2006, the United States Patent and Trademark Office ("PTO") duly, properly and legally issued U.S. Patent No. 7,115,344 ("the '344 patent") entitled "Photomask and Pattern Forming Method Employing the Same" to Renesas as the assignee of inventors Norio Hasegawa, Fumio Murai, and Katsuya Hayano. Renesas has owned the '344 patent since its issuance. A copy of the '344 patent is attached as Exhibit A.

8. On October 3, 2006, the PTO duly, properly and legally issued U.S. Patent No. 7,116,128 ("the '128 patent") entitled "Semiconductor Device With Bus Terminating Function" to Renesas as the assignee of inventor Takashi Kubo. Renesas has owned the '128 patent since its issuance. A copy of the '128 patent is attached as Exhibit B.

Count I: Infringement of the '344 Patent

9. Plaintiff repeats and realleges paragraphs 1-8 above.

10. Defendants infringed, contributed to the infringement by others of, or actively induced infringement by others of the '344 patent by making, using, selling, offering to sell, or causing to be sold products or equipment in the United States, or importing products or equipment into the United States, including but not limited to 512 Mb DDR1, 512 Mb DDR2, and 1 Gb DDR2 SDRAM products, manufactured by a process embodying at least one claimed invention thereof in violation of 35 U.S.C. § 271(a), (b), (c), or (g), and such infringement is continuing. Upon information and belief, Defendants had actual notice of the '344 patent before the filing of this Complaint.

11. Defendants' infringement of the '344 patent has been and continues to be willful, warranting a finding that this is an exceptional case under 35 U.S.C. § 285 and entitling Plaintiff to treble damages and an award of reasonable attorneys' fees.

12. Defendants' past and continuing infringement of the '344 patent has damaged Plaintiff in an amount to be determined, but in no event less than a reasonable royalty.

13. Defendants' continuing infringement of the '344 patent causes Plaintiff to suffer irreparable harm. Upon information and belief, Defendants' infringement will continue unless enjoined by the Court. Plaintiff has no adequate remedy at law and is entitled to a permanent injunction prohibiting Defendants from infringing the '344 patent in violation of 35 U.S.C. §§ 271(a), (b), (c), or (g).

Count II: Infringement of the '128 Patent

14. Plaintiff repeats and realleges paragraphs 1-13 above.

15. Defendants infringed, contributed to the infringement by others of, or actively induced infringement by others of the '128 patent by making, using, selling,

offering to sell, or causing to be sold products or equipment in the United States, including but not limited to 512 Mb DDR2 and 1 Gb DDR2 SDRAM products, embodying at least one claimed invention thereof in violation of 35 U.S.C. § 271(a), (b), or (c), and such infringement is continuing. Upon information and belief, Defendants had actual notice of the '128 patent before the filing of this Complaint.

16. Defendants' infringement of the '128 patent has been and continues to be willful, warranting a finding that this is an exceptional case under 35 U.S.C. § 285 and entitling Plaintiff to treble damages and an award of reasonable attorneys' fees.

17. Defendants' past and continuing infringement of the '128 patent damaged Plaintiff in an amount to be determined, but in no event less than a reasonable royalty.

18. Defendants' continuing infringement of the '128 patent causes Plaintiff to suffer irreparable harm. Upon information and belief, Defendants' infringement will continue unless enjoined by the Court. Plaintiff has no adequate remedy at law and is entitled to a permanent injunction prohibiting Defendants from infringing the '128 patent in violation of 35 U.S.C. §§ 271(a), (b), or (c).

Prayer for Relief

WHEREFORE, Plaintiff prays for entry of a judgment against Defendants as follows:

A. That Defendants infringed the '344 patent;

B. That Defendants and their respective agents, officers, directors, servants, employees, and all persons acting in concert with them, directly or indirectly, be permanently enjoined from infringing, inducing others to infringe, or contributing to the infringement of the '344 patent;

C. That Defendants infringed the '128 patent;

D. That Defendants and their respective agents, officers, directors, servants, employees, and all persons acting in concert with them, directly or indirectly, be permanently enjoined from infringing, inducing others to infringe, or contributing to the infringement of the '128 patent;

E. That Defendants account for and pay to Plaintiff damages adequate to compensate it for defendants' infringement, in an amount to be proven, together with interest and costs as fixed by the Court;

F. That Defendants' infringement has been willful and trebling the award of damages;

G. That this case is exceptional and awarding Plaintiff its costs, expenses, and attorneys' fees in accordance with 35 U.S.C. § 285; and

H. That Plaintiff be awarded such other and further relief as the Court deems just and equitable.

Jury Demand

Plaintiff demands a trial by jury on all issues triable by a jury.

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DATED: January 26, 2007

EXHIBIT A

US007115344B2

(12) **United States Patent**
Hasegawa et al.

(10) **Patent No.: US 7,115,344 B2**
(45) **Date of Patent: Oct. 3, 2006**

(54) **PHOTOMASK AND PATTERN FORMING METHOD EMPLOYING THE SAME**

(75) Inventors: **Norio Hasegawa**, Tokyo (JP); **Fumio Murai**, Tokyo (JP); **Katsuya Hayano**, Hachioji (JP)

(73) Assignee: **Renesas Technology Corp.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 111 days.

(21) Appl. No.: **10/777,060**

(22) Filed: **Feb. 13, 2004**

(65) **Prior Publication Data**

US 2004/0161707 A1 Aug. 19, 2004

Related U.S. Application Data

(60) Continuation of application No. 10/096,599, filed on Mar. 14, 2002, now Pat. No. 6,733,953, which is a continuation of application No. 09/893,532, filed on Jun. 29, 2001, now Pat. No. 6,383,718, which is a continuation of application No. 09/577,367, filed on May 23, 2000, now Pat. No. 6,258,513, which is a continuation of application No. 09/359,732, filed on Jul. 23, 1999, now Pat. No. 6,087,074, which is a continuation of application No. 09/188,368, filed on Nov. 10, 1998, now Pat. No. 6,013,398, which is a continuation of application No. 08/904,754, filed on Aug. 1, 1997, now Pat. No. 5,851,703, which is a continuation of application No. 08/699,732, filed on Aug. 20, 1996, now Pat. No. 5,656,400, which is a continuation of application No. 08/418,402, filed on Apr. 7, 1995, now Pat. No. 5,578,421, which is a division of application No. 08/162,319, filed on Dec. 7, 1993, now Pat. No. 5,429,896.

(30) **Foreign Application Priority Data**

Dec. 7, 1992 (JP) 2004-326433

(51) **Int. Cl.**
G01F 9/00 (2006.01)
G03C 5/00 (2006.01)

(52) **U.S. Cl.** **430/5**; 430/311

(58) **Field of Classification Search** 430/5, 430/311
See application file for complete search history.

(56) **References Cited**

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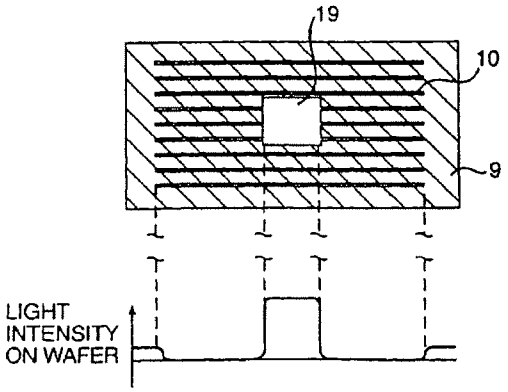
(Continued)

Primary Examiner—S. Rosasco
(74) *Attorney, Agent, or Firm*—Mattingly, Stanger, Malur & Brundidge, P.C.

(57) **ABSTRACT**

A semitransparent phase shifting mask has, in the periphery of a pattern element area, a light shielding portion which is formed by a semitransparent phase shifting portion and a transparent portion with the optimal size combination. A pattern is formed employing the semitransparent phase shifting mask.

19 Claims, 4 Drawing Sheets



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6,660,438	B1 *	12/2003	Tanaka et al.	430/22

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Flanders et al, "Spatial period division—A new technique for exposing submicrometer-line width periodic and quasiperiodic patterns", Journal of Vaccum Science Technology, 16(6), Nov./Dec. 1979, pp. 1949-1952.

* cited by examiner

FIG. 1A

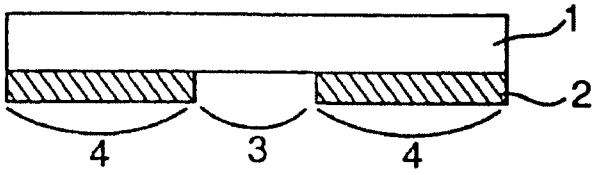

FIG. 1B

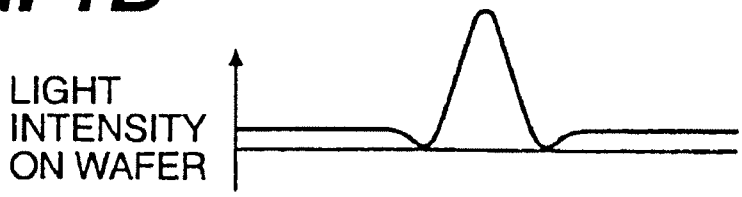

FIG. 2A

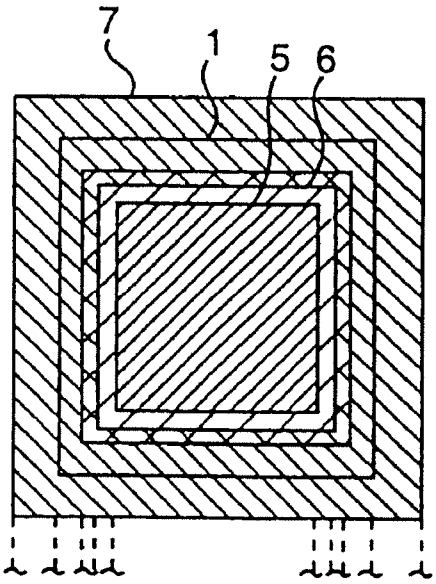

FIG. 2B

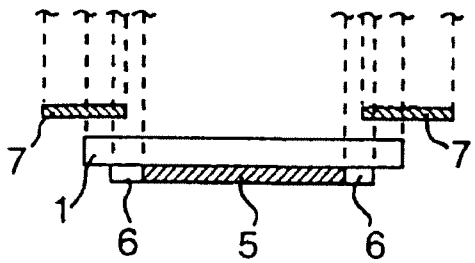

FIG. 3A

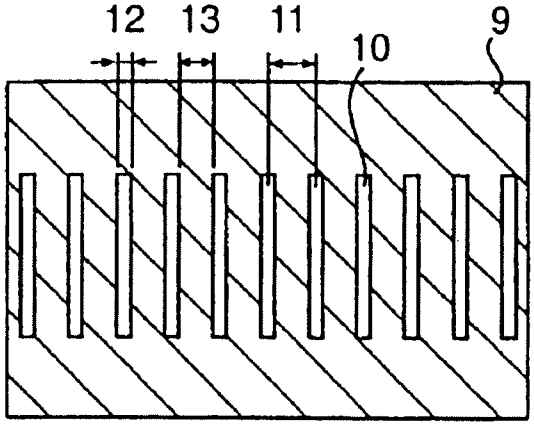
12
13
11
10
9

FIG. 3B

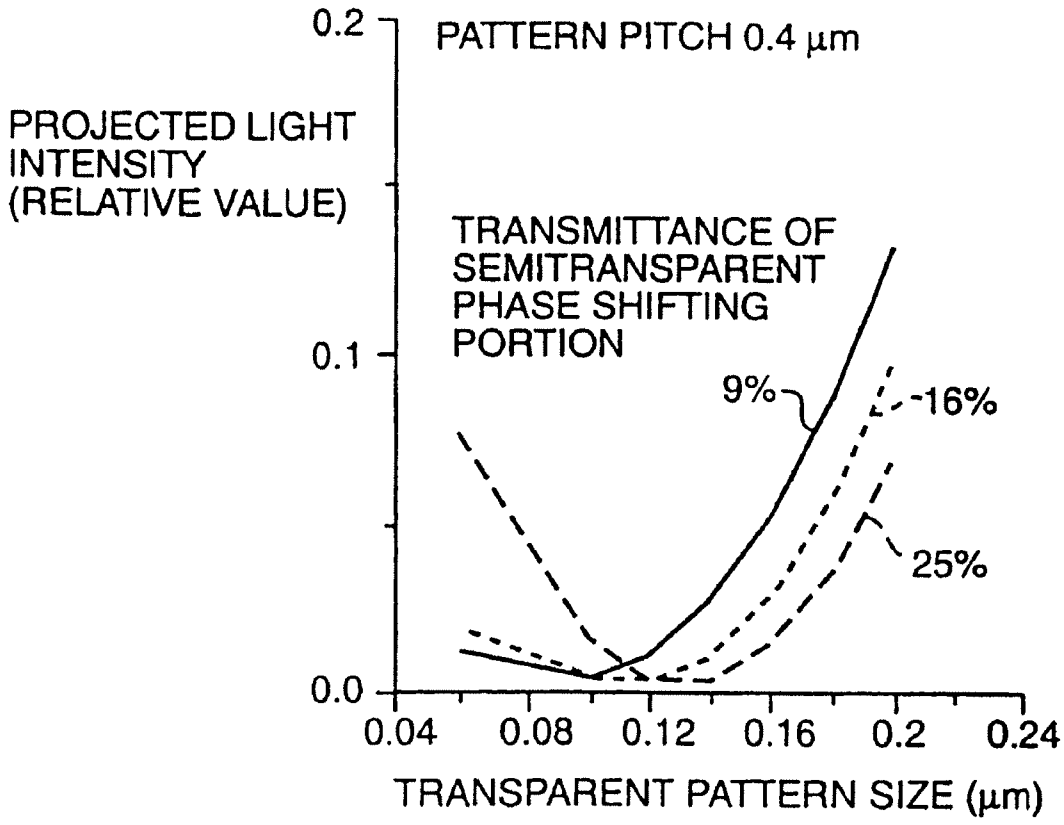
0.2
PATTERN PITCH 0.4 μm
PROJECTED LIGHT INTENSITY (RELATIVE VALUE)
TRANSMITTANCE OF SEMITRANSPARENT PHASE SHIFTING PORTION
9%
16%
25%
0.1
0.0
0.04
0.08
0.12
0.16
0.2
0.24
TRANSPARENT PATTERN SIZE (μm)

FIG. 4

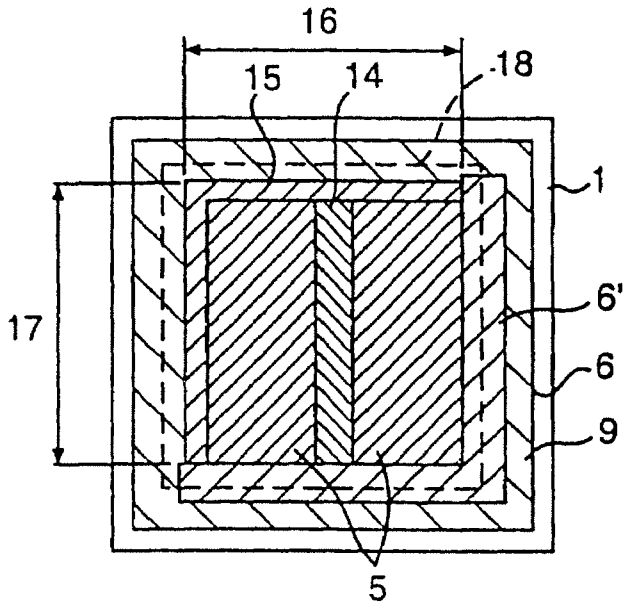

FIG. 5A

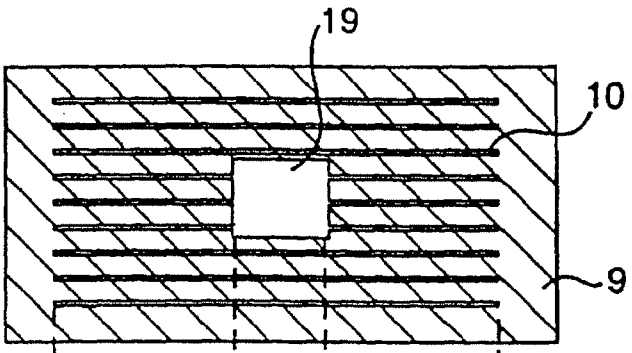

FIG. 5B

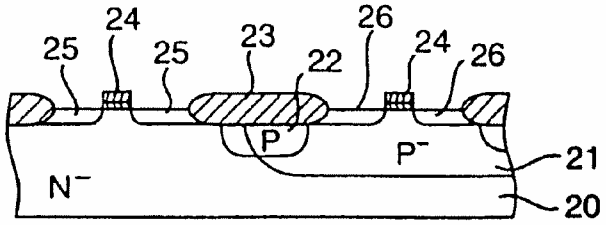

FIG. 6A

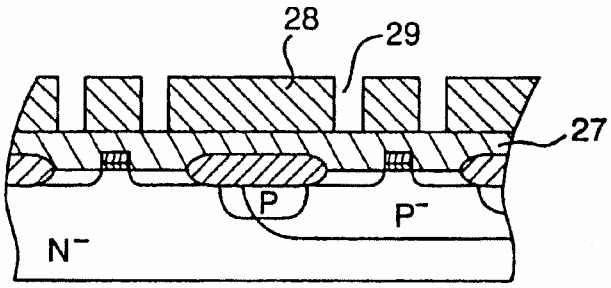

FIG. 6B

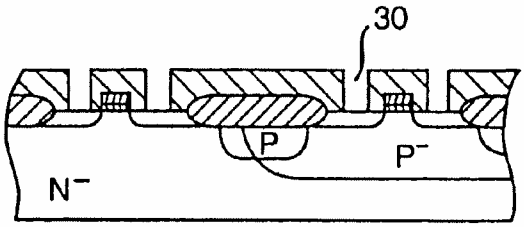

FIG. 6C

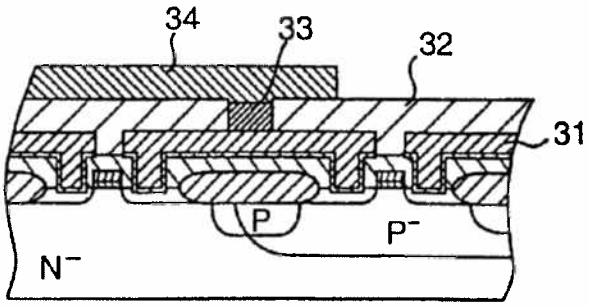

FIG. 6D

PHOTOMASK AND PATTERN FORMING METHOD EMPLOYING THE SAME

This is a continuation application of U.S. Ser. No. 10/096,599, filed Mar. 14, 2002, now U.S. Pat. No. 6,733,953; which is a continuation application of U.S. Ser. No. 09/893,532, filed Jun. 29, 2001, now U.S. Pat. No. 6,383,718; which is a continuation application of U.S. Ser. No. 09/577,367, filed May 23, 2000, now U.S. Pat. No. 6,258,513; which is a continuation application of U.S. Ser. No. 09/359,732, filed Jul. 23, 1999, now U.S. Pat. No. 6,087,074; which is a continuation application of U.S. Ser. No. 09/188,368, filed Nov. 10, 1998, now U.S. Pat. No. 6,013,398; which is a continuation application of U.S. Ser. No. 08/904,754, filed Aug. 1, 1997, now U.S. Pat. No. 5,851,703; which is a continuation application of U.S. Ser. No. 08/699,732, filed Aug. 20, 1996, now U.S. Pat. No. 5,656,400; which is a continuation application of U.S. Ser. No. 08/418,402, filed Apr. 7, 1995, now U.S. Pat. No. 5,578,421; which is a divisional application of U.S. Ser. No. 08/162,319, filed Dec. 7, 1993, now U.S. Pat. No. 5,429,896.

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to a photomask which is used to manufacture a semiconductor device and the like, and more particularly to a photomask which has been subjected to a processing of shifting a phase of exposure light beams and a pattern forming method employing the same.

Along with an increase of the integration scale for semiconductor devices, sizes of patterns for forming constituent elements of the devices become fine, and size equal to or smaller than the critical resolution of a projection aligner are required. As a method of fulfilling such a request, in JP-B-62-50811 published on Oct. 27, 1987, and corresponding to JP-A-57-62052 (laid open on Apr. 14, 1982) for example, a photomask is employed in which a transparent film for shifting a phase of exposure light beams is provided on a transparent portion on one of the opposite sides sandwiching an opaque portion, and thus the resolution of a pattern is exceptionally improved.

In the above-mentioned prior art, a phase shifter needs to be arranged in one of the transparent portions adjacent to each other, and for the arrangement of the phase shifter in the complicated element pattern, high trial and error is necessarily required. Thus, there is required considerable labor. In addition, since the number of processes of manufacturing a photomask is doubled as compared with the prior art, the reduction in yield and the increase in cost become problems.

Those problems can be settled by employing a semitransparent phase shifting mask in which a semitransparent portion and a transparent portion are provided, and some of the light beams passed through the semitransparent portion are phase-inverted with respect to light beams having passed through the transparent portion. With respect to this point, the description will hereinbelow be given with reference to the accompanying drawings.

FIG. **1**A is a cross sectional view showing a structure of an example of a semitransparent phase shifting mask. In the figure, reference numeral **1** designates a transparent substrate, and a reference numeral **2** designates a semitransparent film. A thickness of the semitransparent film **2** is adjusted such that the light beams having passed through the transparent portion **3** are phase-inverted with respect to the light beams having passed through a semitransparent portion **4**. The semitransparent film **2** has a transmittance such that a light beam having passed through the transparent substrate **1** and the semitransparent film **2** has an intensity high enough to cause interference with a light beam having passed through the transparent substrate **1**. The transparent film used in this specification means a film having the above-mentioned transmittance.

The light intensity distribution of the projected light beams on a wafer becomes, as shown in FIG. **1**B, a sharp light intensity distribution. The reason such a sharp light intensity distribution is obtained is that, since the light beams having passed through the transparent portion are phase-inverted with respect to the light beams having passed through the semitransparent portion, the former and the latter cancel each other in a boundary portion of the pattern so that the light intensity becomes approximately zero. In addition, since the intensity of the light beams having passed through the semitransparent portion is adjusted to be equal to or lower than the sensitivity of a photoresist, the intensity of the light beams having passed through the semitransparent portion is not an obstacle to the formation of the pattern. That is, in this method, since the phase inversion effect between the pattern to be transferred and the semitransparent portion therearound is utilized, there is no need to take, as in the normal phase shifting mask, the arrangement of the phase shifter into consideration. In addition, in the prior art phase shift mask, the two lithography processes are required for the formation of the mask. However, in this method, one lithography process has only to be performed. Thus, it is possible to form the mask very simply.

In this method, the light beams, which have an intensity that is equal to or lower than the sensitivity of a photoresist to which the pattern of the mask is to be transferred, are made to pass through the semitransparent film so that the light beams which have passed through the semitransparent film are phase-inverted with respect to the light beams which have passed through the transparent portion, and thus, the contrast of the pattern is improved. As a result, it is possible to improve the resolution of an aligner for transferring the mask pattern. The basic principle of the semitransparent phase shifting mask is described in D. C. Flanders et al.: "Spatial Period Division—A New Technique for Exposing Submicrometer—Linewidth Periodic and Quasiperiodic Patterns" J. Vac. Sci. Technol., 16(6), November/December pp 1949 to 1952 (1979), U.S. Pat. Nos. 4,360,586 and 4,890,309 and JP-A-4-136854 (laid open on May 11, 1992).

In the lithography process in which the above-mentioned semitransparent phase shifting mask is employed, in the normal exposed area, good pattern formation can be performed. However, it has been made clear by the investigations made by the present inventors that since in the actual exposure of the wafer, the mask pattern is repeatedly transferred by step-and-repeat exposure, the light beams which have leaked from the semitransparent area, which is located outside the periphery of the actual pattern element corresponding to an active region of a substrate, leak out to the adjacent exposed area, and thus this is an obstacle to good pattern formation.

It is therefore an object of the present invention to provide a photomask by which a good pattern can be obtained even in the case of an exposure, in which a mask pattern is repeatedly transferred by step-and-repeat exposure, and a pattern forming method employing the same.

According to one aspect of the present invention, the above-mentioned object can be attained by effectively making a light-shielding or opaque area of a semitransparent

phase shift mask which is located outside the periphery of a pattern element formation area of the semitransparent phase shifting mask.

These and other objects and many of the attendant advantages of the invention will be readily appreciated as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and 1B are respectively a cross-sectional view showing a structure of a semitransparent phase shifting mask, and a view showing the light intensity distribution of projected light beams on a wafer when using the mask shown in FIG. **1**A.

FIGS. **2**A and 2B are respectively a plan view and a cross sectional view each showing a structure of a photomask according to the present invention.

FIG. **3**A is a plan view showing a structure of a light shielding portion of the photomask according to the present invention.

FIG. **3**B is a graphical representation showing the relationship between the size of a transparent pattern of the photomask according to the present invention and the intensity of projected exposure light beams.

FIG. **4** is a plan view showing a structure of a mask for forming contact holes of a 64 Mbit-DRAM according to the present invention.

FIGS. **5**A and 5B are respectively a plan view showing a structure of a window pattern portion for aligning the position of the mask according to the present invention, and a view showing the light intensity distribution of the projected light beams on the wafer when using the mask shown in FIG. **5**A.

FIGS. **6**A through 6D are cross sectional views showing steps of a process of manufacturing a semiconductor device according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

A first embodiment of the present invention will hereinafter be described in detail. FIGS. **2**A and 2B are respectively a plan view and a cross sectional view each showing the appearance of a photomask employed in the present embodiment. In those figures, reference numeral **1** designates a transparent substrate, and reference numeral **5** designates an element pattern portion in which both a semitransparent phase shifting portion and a transparent portion are arranged. Moreover, reference numeral **6** designates a portion acting, on a wafer, as a light shielding portion in which semitransparent phase shifting patterns are arranged at a pitch equal to or smaller than the resolution.

Reference numeral **7** designates a masking blade for shielding, on the aligner side, the exposure light beams. Since the masking blade **7** is poor in positional accuracy, it is positioned so as to shield the light beams passing through the portion which is located outside the intermediate position of the width of the area **6** acting as the light shielding portion.

The details of the area **6** acting as the light shielding portion will hereinbelow be described with reference to FIGS. **3**A and 3B. FIG. **3**A is a plan view showing a structure of a pattern. In this connection, each transparent pattern

portion **10** is formed within a semitransparent phase shifting portion **9**. An arrangement pitch **11** of the transparent patterns **10** is determined depending on the resolution characteristics of the projection optical system employed. The arrangement pitch P is expressed by the following expression: $P=\alpha\cdot\lambda/NA$, where NA represents a numerical aperture of a projection lens, λ represents a wavelength of the exposure light beams, and α represents a coefficient.

In this connection, on the basis of the experiments made by the present inventors, it is desirable that the coefficient α is set to a value equal to or smaller than 0.8. However, the optimal value of α is not limited thereto or thereby because the optimal value of α depends on the characteristics of the illuminating system, the pattern configuration and the like.

The width **12** of the transparent pattern **10** influences largely the formation of a dark portion. When both a semitransparent phase shifting pattern and a transparent pattern are arranged with the same size and at a pitch equal to or lower than the critical resolution, a pattern image can be erased. But, in this case, the resulting uniform light intensity does not become zero. This reason is that since there is a difference between the quantity of light beams having passed through the semitransparent phase shifting portion and that of light beams having passed through the transparent portion, the function of cancelling those light beams each other due to the phase inversion effect is not efficiently performed. Then, when the ratio of the area of the semitransparent phase shifting portion to that of the transparent portion is adjusted in accordance with a set transmittance of the semitransparent phase shifting portion, it is made clear that the light intensity can be zero.

FIG. **3**B shows the intensity of the projected light beams which is obtained on the wafer when changing the width **12** of the transparent pattern **10**. The intensity of the projected light beams shows the intensity of the light beams which have passed through the pattern of FIG. **3**A. The pitch of the transparent patterns **10** was determined to be 0.4 μm by using $\alpha=0.1$ in the expression of the arrangement pitch.

With respect to the three kinds of transmittance 9%, 16% and 25% of the semitransparent phase shifting portion, the change in the intensity of the projected light beams were examined by changing the size of the transparent pattern **10**. The axis of abscissa of the graph represents the size of the transparent pattern **10**. From the graph of FIG. **3**B, it can be seen that a minimum value is present in the intensity of the projected light beams depending on the size of the transparent pattern, and this local minimum value is variable depending on the transmittance of the semitransparent phase shifting portion. That is, it can be seen that in accordance with the transmittance of the semitransparent phase shifting portion **9**, an optimal transparent pattern size can be found.

Denoting the size ratio of size **12** of the transparent pattern to the size **13** of the semitransparent phase shifting portion **13** by α, an optimal value thereof will be expressed by the following expression: $\alpha=\beta\cdot\sqrt{T}$, where T represents a transmittance of the semitransparent phase shifting portion, and β represents a coefficient. The allowable intensity of the projected light beams is variable depending on the intended purpose. In the case of preventing exposure of a photoresist due to a double exposure, the allowable intensity of the projected light beams may be set to about one-half the intensity of light which has passed through the semitransparent phase shifting portion. However, in the case of preventing a double exposure of a dark portion with a fine pattern containing portion, the change in the size of the fine pattern needs to be reduced as much as possible, and thus it is desirable that the allowable intensity of the projected light

beams is set to a value equal to or lower than 0.05. The value of β in this case is in the range of about 0.5 to about 2.0.

Then, the area **6** of FIG. **2**A was formed on the basis of the optimal conditions thus obtained, and by actually using the projection aligner, the pattern element **5** corresponding to the active region was exposed by the step-and-repeat process. As a result, a good pattern element corresponding to the active region could be formed without pattern destruction and size shifting even in the area in which the area **6** was double-exposed.

As described above, the semitransparent phase shifting portion and the transparent portion were formed with the optimal size combination, whereby the effective dark portion could be formed. Incidentally, although in the present embodiment, the example is shown in which the line transparent pattern is formed in the semitransparent phase shifting area, the present invention is not limited thereto or thereby. That is, for example, there is particularly no problem even in the case of an island-like pattern and other patterns. In such cases, if a in the expression $\alpha=\beta\cdot\sqrt{T}$ is replaced with the area ratio of the area of the transparent pattern to the area of the semitransparent phase shifting portion, substantially the same effects can be obtained.

In addition, in the present embodiment, the combination of the semitransparent phase shifting pattern and the transparent pattern is applied to prevent the double exposure. However, this application of the present invention is not limited thereto or thereby. It is, of course, to be understood that the combination is applicable to the necessary portions such as a window pattern for aligning the mask position, a pattern for detecting the wafer position, and a semitransparent phase shifting portion having a large area, all of which require a dark portion. Further, the above-mentioned photomask having a light shielding portion is useful for pattern formation when manufacturing a semiconductor device.

Incidentally, the above-mentioned light shielding portion is applicable to the formation of a light shielding portion in a pattern element region of a substrate. In this case, since the ratio of the transmittance of the transparent portion to that of the light shielding portion can be made large, it is possible to increase the tolerance for the variation of the quantity of light beams required for the exposure.

As for the materials used for the formation of the semitransparent phase shifting portion, a lamination film of a semitransparent metal film (made of chromium, titanium or the like) or a silicide film (e.g., a molybdenum silicide film) and a silicon oxide film for the phase shift, or a single layer film such as a metal oxide film (e.g., a chromium oxide film) or metal nitride film (e.g., a chromium nitride film) may be employed. In the case where a single layer film such as a chromium oxide film or a chromium nitride film is employed, since the refractive index thereof is larger than that of the silicon oxide film, the film can be thinned. As a result, since the influence of the light diffraction can be reduced, this single layer film is suitable for the formation of a fine pattern.

Embodiment 2

A second embodiment of the present invention will hereinafter be described with reference to FIG. **4**. FIG. **4** is a plan view showing a structure of a photomask which is used to form contact holes of a 64 Mbit-dynamic random access memory (DRAM). Two DRAM element areas **5** are arranged in a transparent substrate **1**. A scribing area **14** is provided between the two pattern element areas **5**. In addition, in a peripheral scribing area **15** on two sides perpendicular to each other, a pattern for measuring the accuracy of the mask alignment, a target pattern for the mask alignment, and the like are arranged, which becomes necessary for the process of manufacturing a device.

In the two sides opposite to the other sides of the scribing area, a pattern configuration **6'** of light shielding portion **6** of the present invention is arranged. The step-and-repeat process in the projection aligner is performed at a pitch **16** in the transverse direction and at a pitch **17** in the longitudinal direction. The peripheral portion which is located outside a dotted line **18** as the setting center is mechanically shielded from the light beams by a mechanical light shielding plate of the aligner. In this connection, the dotted line **18** is set at a distance equal to or longer than the positional accuracy of the mechanical light shielding plate from the scribing area such that the mechanical light shielding plate is not shifted to the scribing area by mistake. In addition, the width of the pattern configuration **6'** is set to a value equal to or larger than the positional accuracy of the mechanical light shielding plate, and the dotted line **18** is arranged in about the central portion of the pattern configuration **6'**. Further, at least three of the four corner portions have pattern configurations.

As a result of using this photomask in order to manufacture the 64 Mbit-DRAM, the double exposure in the periphery of the chip can be perfectly prevented, and thus a good device can be manufactured. In addition, in the case where the pattern element area **5** is formed by one chip, or the photomask having the pattern configuration **6'** is applied to devices other than DRAM, the same effects can be obtained.

Further, a description will hereinbelow be given with respect to an example in which the pattern configuration **6'** of the present invention is arranged in the periphery of a window pattern which is used to align the mask position with reference to FIGS. **5**A and **5**B. FIG. **5**A is a plan view showing a structure of the window pattern portion which is used to align the mask position. FIG. **5**B shows the distribution of the light intensity on the wafer corresponding to the mask position.

As shown in FIG. **5**A, a transparent portion **10** which has a size fulfilling the conditions for forming the dark portion of FIG. **3**B is formed around a window pattern **19**. It can be seen that in the distribution of the light intensity on the wafer of the photomask of FIG. **5**A at that time, the light intensity in the periphery of the window pattern is, as shown in FIG. **5**B, zero, and thus signals representing the window pattern are obtained with a high signal-to-noise (S/N) ratio and the judgment of the position is performed with accuracy. In such a way, the light shielding pattern configuration of the present invention is applicable to a pattern utilizing light intensity signals each having a high S/N ratio from a mask pattern and other patterns requiring the light shielding portion, as well as to the light shielding in the periphery of a device chip.

Embodiment 3

Hereinbelow, an example will be shown in which a semiconductor device is manufactured according to the present invention. FIGS. **6**A through **6**D are cross sectional views showing steps of a process of manufacturing a semiconductor device. By using the conventional method, a P type well layer **21**, a P type layer **22**, a field oxide film **23**, a polycrystalline Si/SiO_2 gate **24**, a high impurity concentration P type diffusion layer **25**, a high impurity concentration N type diffusion layer **26**, and the like are formed in an N— type Si substrate **20**.

Next, by using the conventional method, an insulating film **27** made of phosphor silicate glass (PSG) is deposited thereon. Then, a photoresist **28** is applied thereto, and a hole pattern **29** is formed by using the semitransparent phase shifting mask of the present invention (refer to FIG. **6**B).

Next, an insulating film **27** is selectively etched by dry etching with the resultant photoresist as an etching mask, thereby to form contact holes **30** (refer to FIG. **6**C). Then, by using the conventional method, a W/TiN electrode wiring **31** is formed, and an interlayer insulating film **32** is also formed.

Next, a photoresist is applied thereto, and then by using a conventional method, a hole pattern **33** is formed using the semitransparent phase shifting mask of the present invention. Then, a W plug is plugged in the hole pattern **33** to connect a second level Al wiring **34** thereto (refer to FIG. **6**D). In a subsequent passivation process, the conventional method is employed.

Incidentally, in the present embodiment, only the main manufacturing processes have been described. In this connection, the same processes as those of the conventional method are employed except that the semitransparent phase shifting mask of the present invention is used in the lithography process of forming the contact hole. By the above-mentioned process, CMOS LSI chips can be manufactured at a high yield.

As set forth hereinabove, according to the present invention, it is possible to prevent the double exposure on the wafer, and a pattern of constituent elements as desired can be formed. By forming the semitransparent phase shifting portion and the transparent portion with the optimal size combination, even if a light-shielding film is not newly formed, the effective dark portion can be formed. In addition, without increasing the number of processes of forming the mask, the semitransparent phase shifting mask can be produced. Further, as a result of manufacturing the semiconductor device by using the photomask of the present invention, it is possible to form a pattern in which the effects inherent in the semitransparent phase shifting mask are sufficiently utilized, without any problem in the double exposure portion, and also it is possible to realize the reduction of the device area.

It is further understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a phase shifting mask including (a) an element forming area having a semitransparent phase shifting film, and (b) a light shielding area provided at a peripheral edge of said element forming area and serving to make an intensity of light having passed through said light shielding area smaller than an intensity of light having passed through said semitransparent phase shifting film, as measured on a to-be-exposed photoresist film, and said light shielding area further including a target pattern for mask aligning; and

transmitting, with a projection exposure optical system, a pattern formed element forming area of said phase shifting mask onto said photoresist film.

2. A method of manufacturing a semiconductor device according to claim **1**, wherein said light shielding area includes a scribing area.

3. A method of manufacturing a semiconductor device according to claim **2**, wherein said target pattern for mask aligning is disposed at said scribing area.

4. A method of manufacturing a semiconductor device according to claim **1**, wherein said phase shifting mask includes a plurality of said element forming area.

5. A method of manufacturing a semiconductor device according to claim **1**,

wherein said light shielding area includes a semitransparent phase shifting pattern having a semitransparent phase shifting portion and a transparent portion.

6. A method of manufacturing a semiconductor device according to claim **1**,

wherein a ratio α of an area of said transparent portion to an area of said semitransparent phase shifting portion is defined as $\alpha=\beta\cdot\sqrt{T}$, where T represents a transmittance of said semitransparent phase shifting portion, and β is in a range of $0.5\leqq\beta\leqq2.0$.

7. A method of manufacturing a semiconductor device according to claim **1**,

wherein the peripheral edge is double-exposed in said transmitting step.

8. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a phase shifting mask including (a) an element forming area having a first semitransparent phase shifting film having a transmittance with respect to exposure light not higher than 25%, and (b) a light shielding area provided at a peripheral edge of said element forming area and serving to make an intensity of light having passed through said light shielding area smaller than an intensity of light having passed through said semitransparent phase shifting film, as measured on a to-be-exposed photoresist film, and said light shielding area further including a target pattern for mask aligning;

preparing a semiconductor substrate at which said photoresist film to be exposed is formed; and

transmitting, with a projection exposure optical system, a pattern formed element forming area of said phase shifting mask onto said photoresist film.

9. A method of manufacturing a semiconductor device according to claim **8**, wherein said light shielding area includes a scribing area.

10. A method of manufacturing a semiconductor device according to claim **9**, wherein said target pattern for mask aligning is disposed at said scribing area.

11. A method of manufacturing a semiconductor device according to claim **8**, wherein said phase shifting mask includes a plurality of said element forming area.

12. A method of manufacturing a semiconductor device according to claim **8**, wherein said light shielding area includes a semitransparent phase shifting pattern having a semitransparent phase shifting portion and a transparent portion.

13. A method of manufacturing a semiconductor device according to claim **12**,

wherein a ratio α of an area of said transparent portion to an area of said semitransparent phase shifting portion is defined as $\alpha=\beta\cdot\sqrt{T}$, where T represents a transmittance of said semitransparent phase shifting portion, and β is in a range of $0.5\leqq\beta\leqq2.0$.

14. A method of manufacturing a semiconductor device according to claim **8**,

wherein the peripheral edge is double-exposed in said transmitting step.

15. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a transparent phase shifting mask including (a) a hole formation semitransparent phase shifting film formed at an element forming area on a photomask substrate, and (b) a light shielding area provided at a peripheral edge portion of said element forming area and serving to make an intensity of light having passed through said light shielding area smaller than an intensity of light having passed through said semitransparent phase shifting film, as measured on a to-be-exposed photoresist film, said light shielding area further including a target pattern for mask aligning; and

exposing, with a projection exposure optical system, a hole pattern formed on said element forming area of said phase shifting mask onto said photoresist film.

16. A method of manufacturing a semiconductor device according to claim 15, wherein said light shielding area includes a scribing area.

17. A method of manufacturing a semiconductor device according to claim 16, wherein said target pattern for mask aligning is disposed at said scribing area.

18. A method of manufacturing a semiconductor device according to claim 15, wherein said phase shifting mask includes a plurality of said element forming area.

19. A method of manufacturing a semiconductor device according to claim 15, wherein a transmittance of said semitransparent phase shifting film with respect to exposure light is not higher that 25%.

* * * * *

EXHIBIT B

US007116128B2

(12) **United States Patent**
Kubo

(10) **Patent No.: US 7,116,128 B2**
(45) **Date of Patent: Oct. 3, 2006**

(54) **SEMICONDUCTOR DEVICE WITH BUS TERMINATING FUNCTION**

(75) Inventor: **Takashi Kubo**, Hyogo (JP)

(73) Assignee: **Renesas Technology Corp.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/212,743**

(22) Filed: **Aug. 29, 2005**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

Oct. 23, 2002 (JP) 2002-307961

(51) **Int. Cl.**
H03K 17/16 (2006.01)

(52) **U.S. Cl.** **326/30**; 326/87

(58) **Field of Classification Search** 326/30, 326/32, 38, 83, 87
See application file for complete search history.

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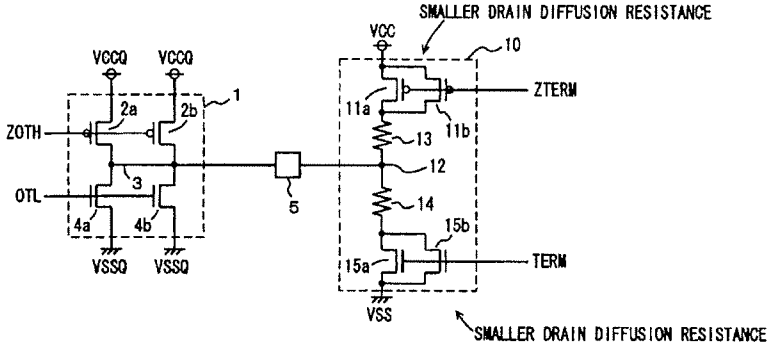
Primary Examiner—Linh Nguyen
(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

The distance between a drain contact and gate electrode in a terminating transistor, which couples a termination resistor connected to an output terminal to a power source node, is set shorter than in an output transistor, which drives an output node in accordance with an internal signal. The area of the terminating circuit is reduced while the reliability against the surge is maintained. Thus, an output circuit containing the terminating circuit that occupies a small area and is capable of transmitting a signal/data at high speed is provided.

11 Claims, 17 Drawing Sheets



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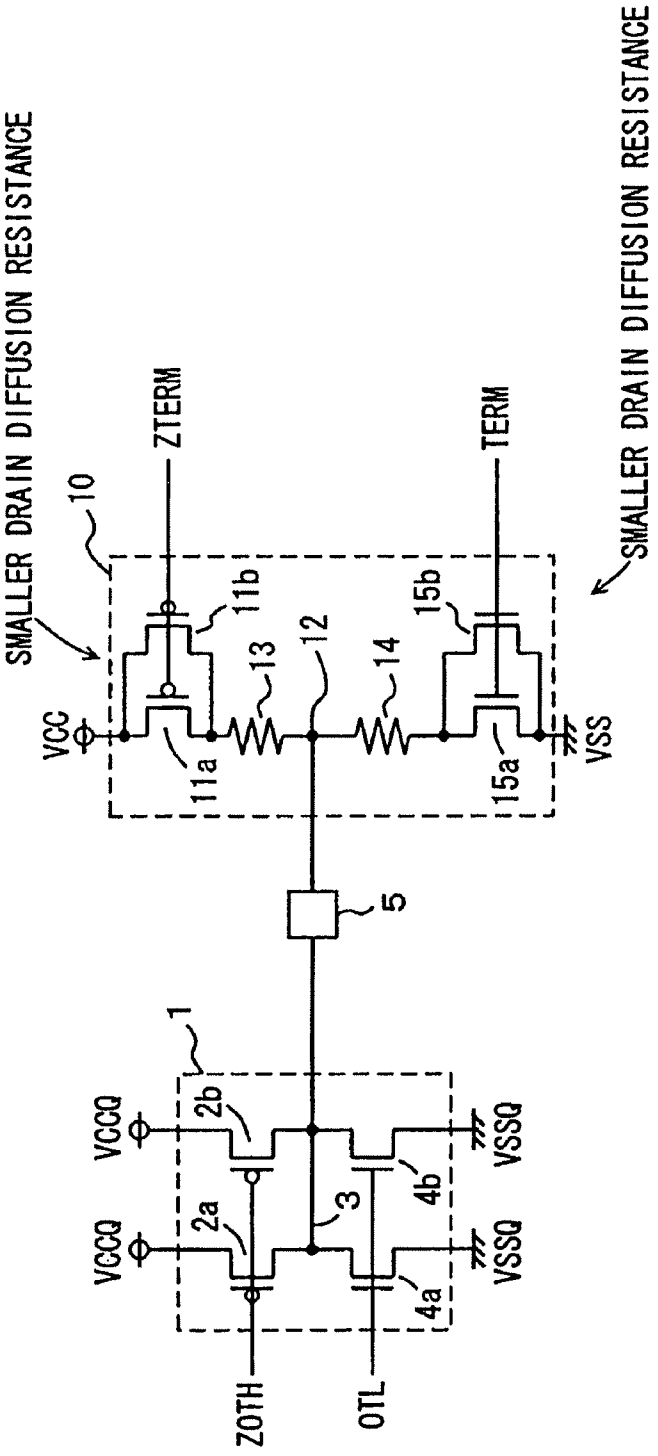
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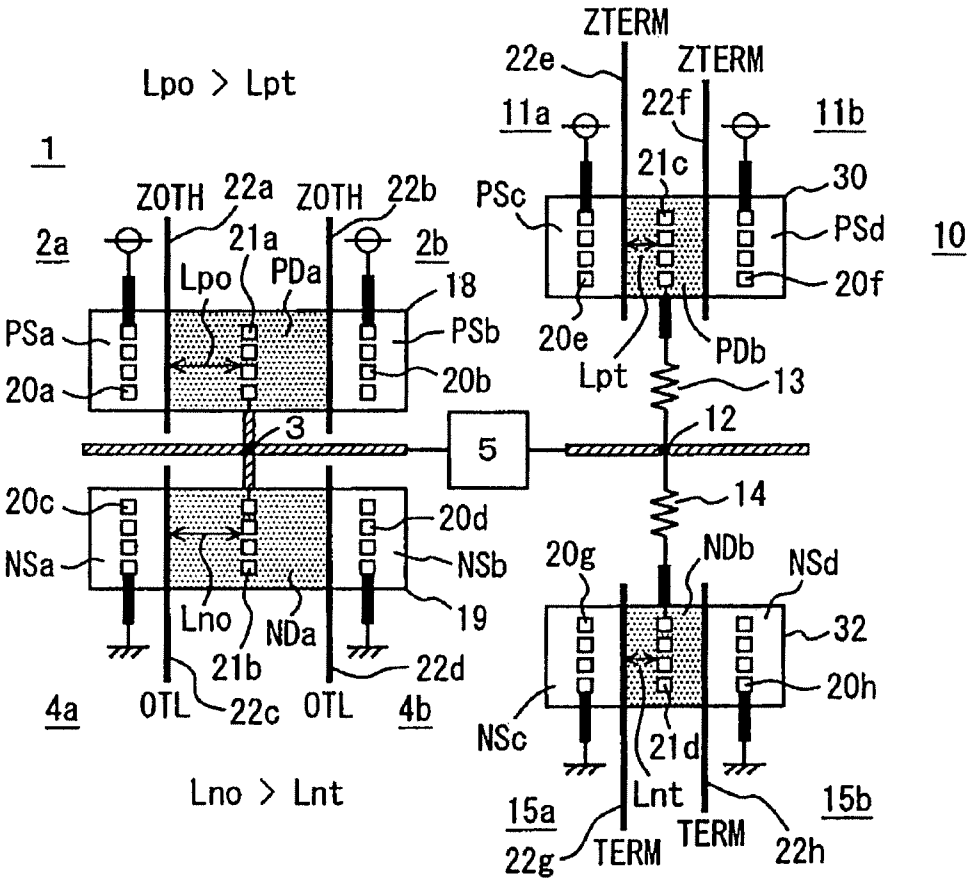
FIG.1

FIG.2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NSa
NSb
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NDa
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21b
22d
4a
OTL
22c
OTL
4b
Lno > Lnt
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22e
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11b
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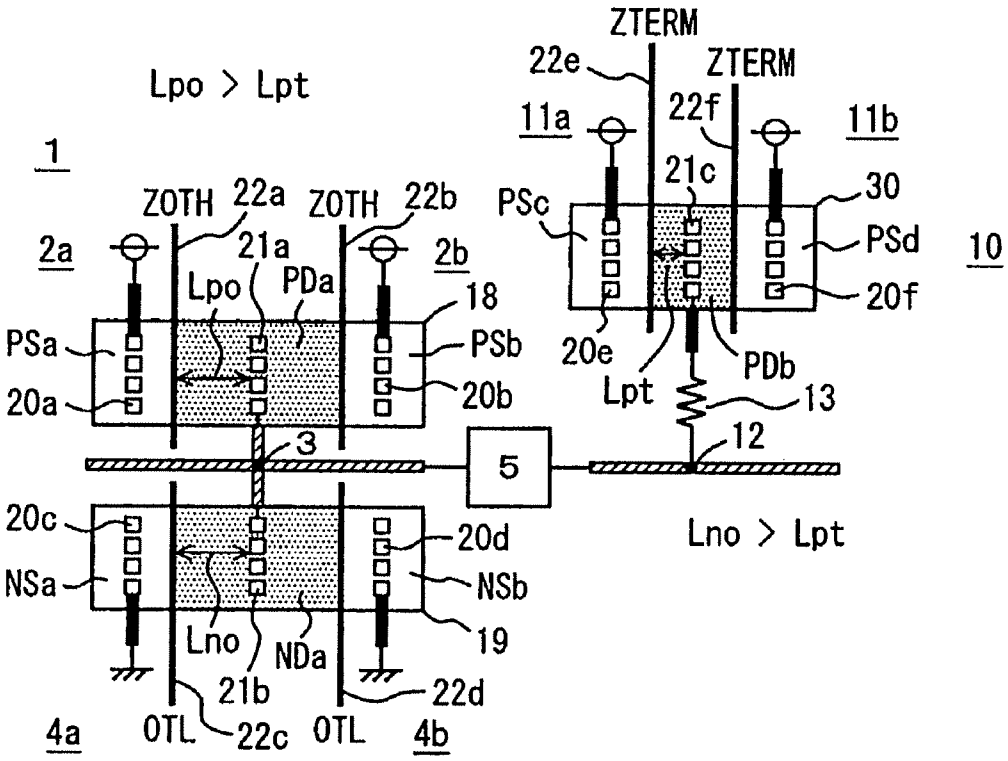
FIG.3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NSb
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22d
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OTL
4b
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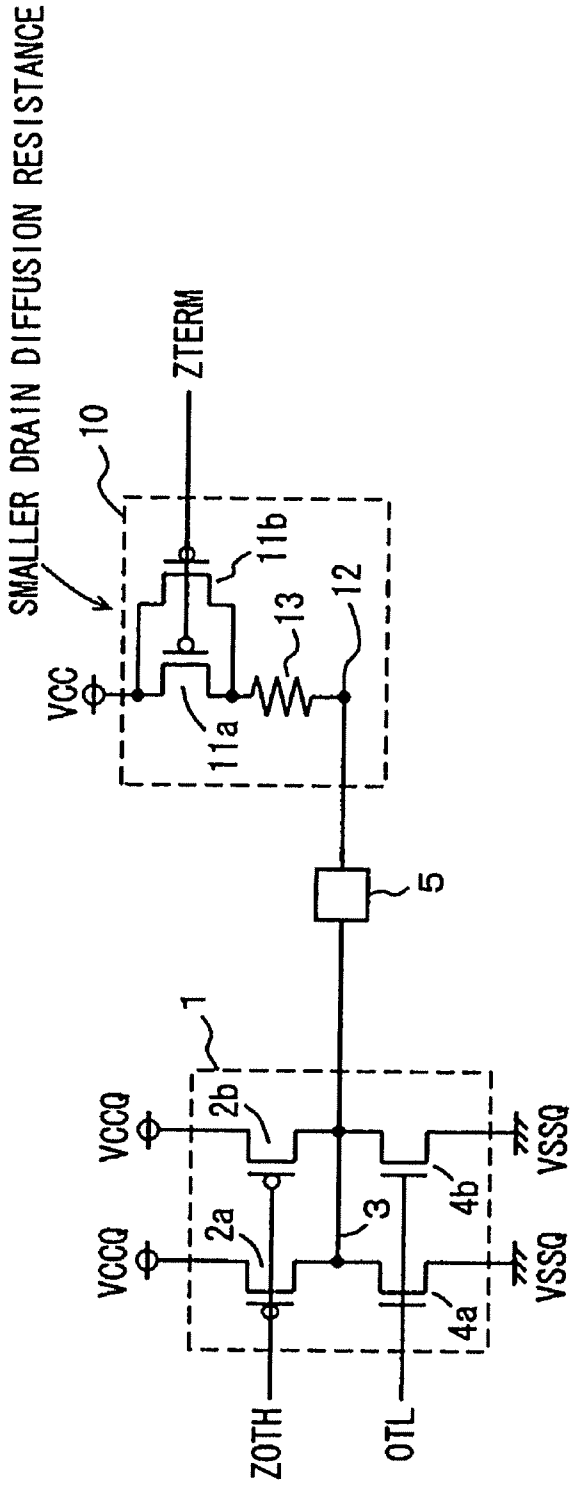
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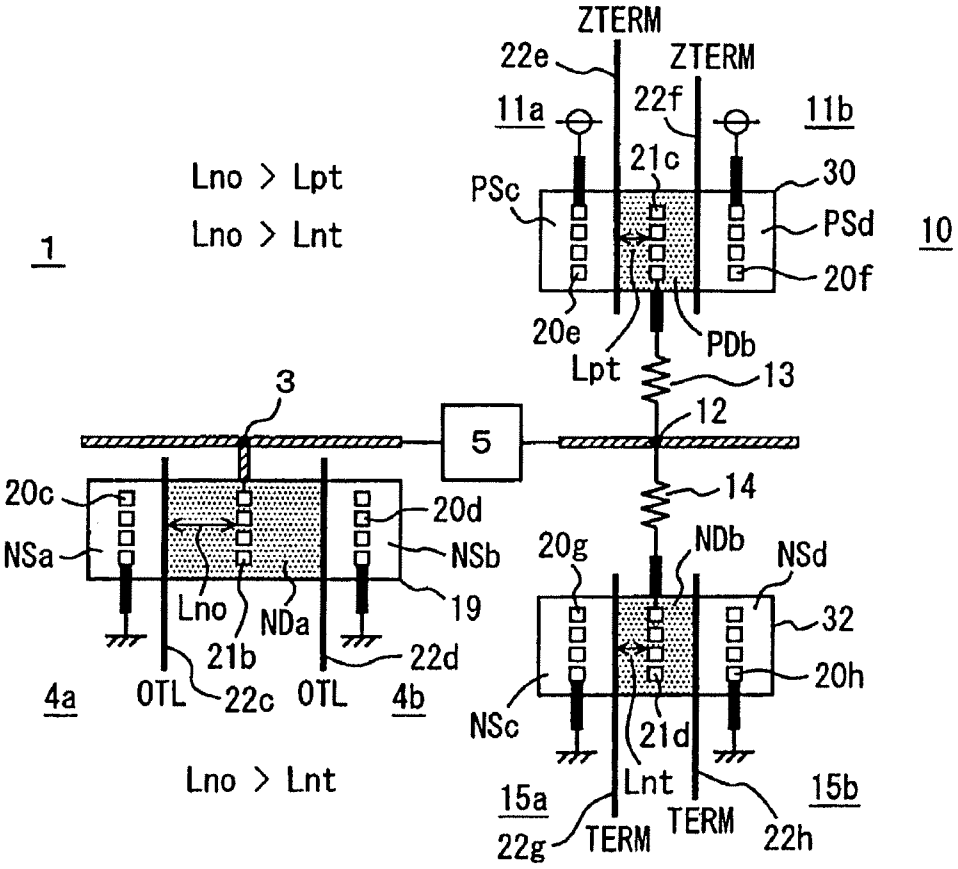
OTL

FIG.4

FIG.5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20c
20d
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NSb
20g
NDb
NSd
19
Lno
NDa
32
21b
22d
20h
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TERM
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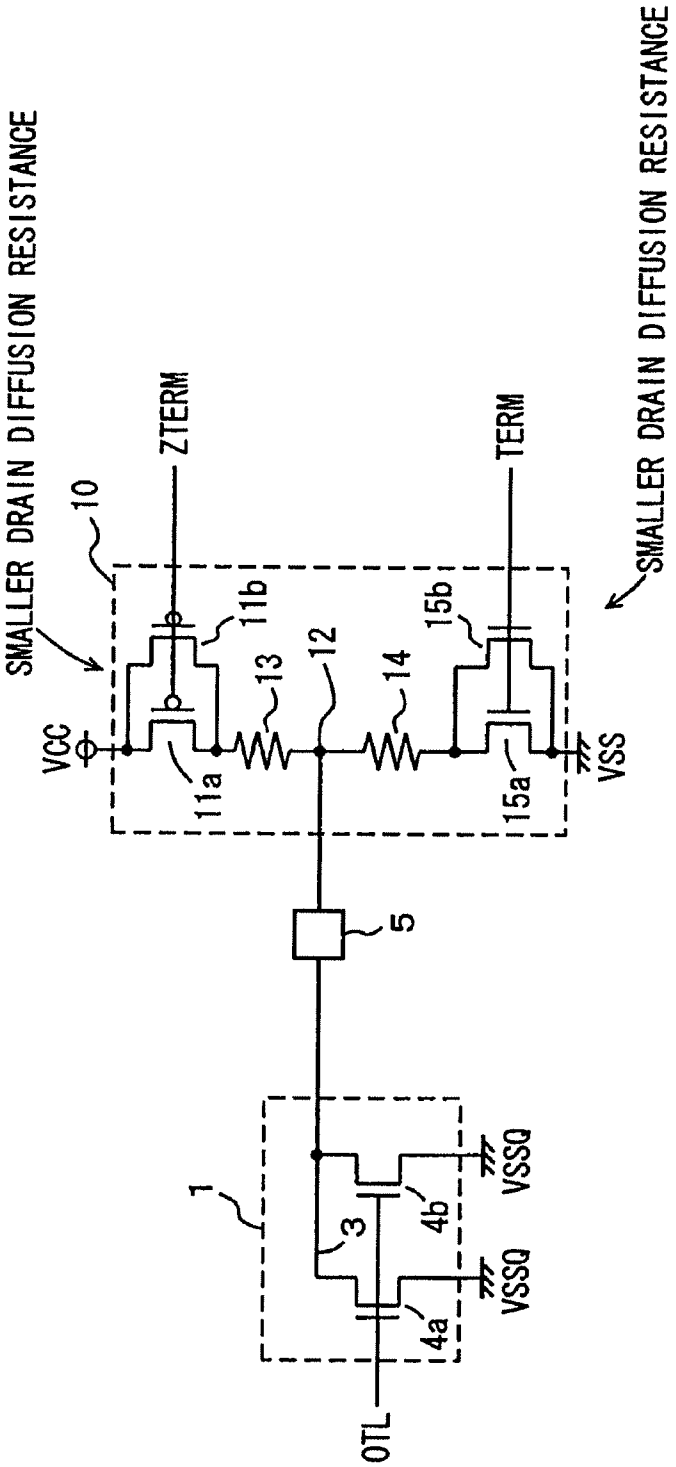
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SMALLER DRAIN DIFFUSION RESISTANCE
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14
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VSSQ
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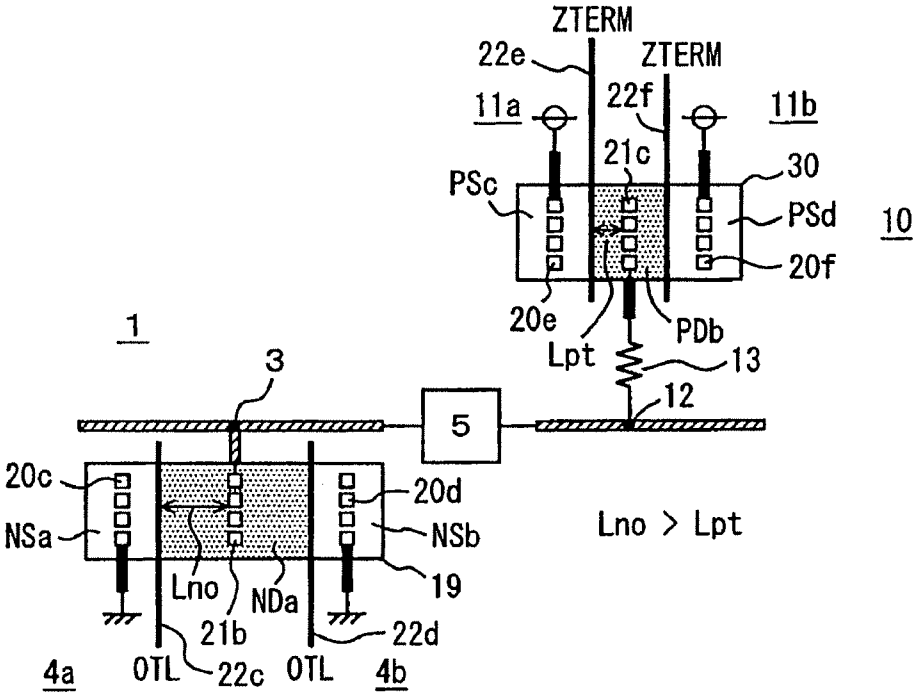
FIG.6

FIG.7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4a
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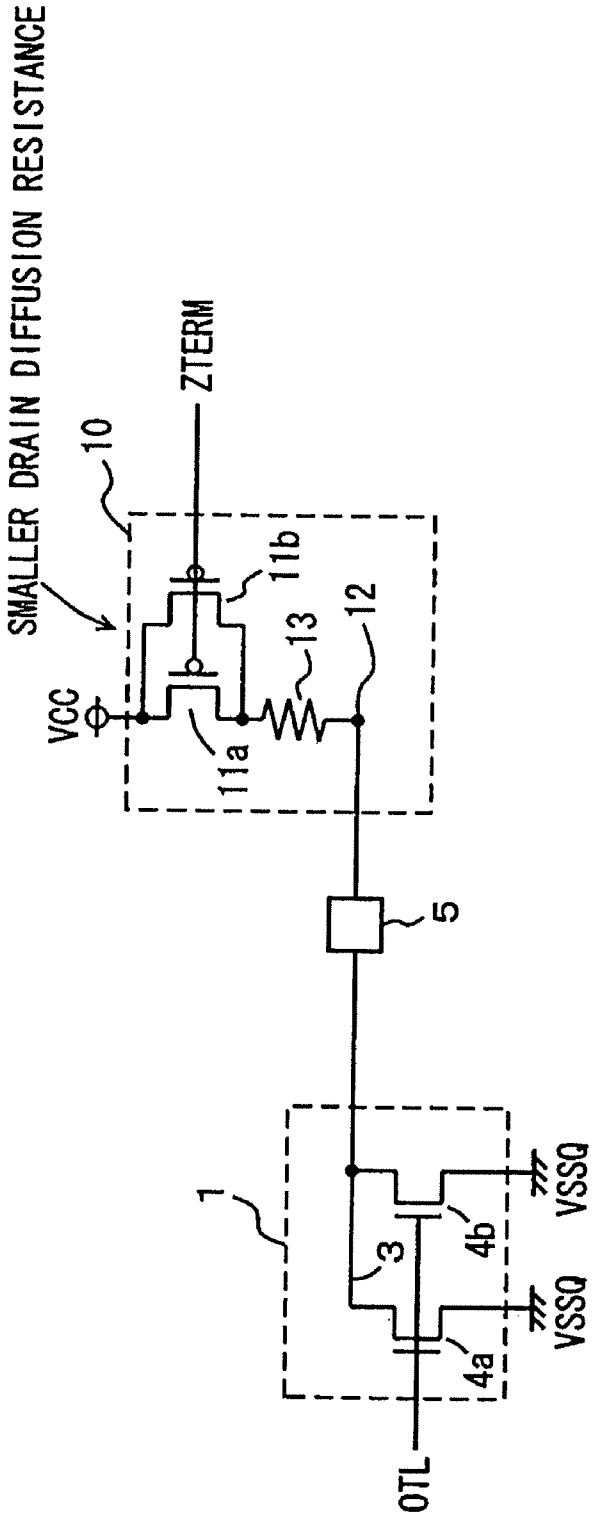
OTL
4b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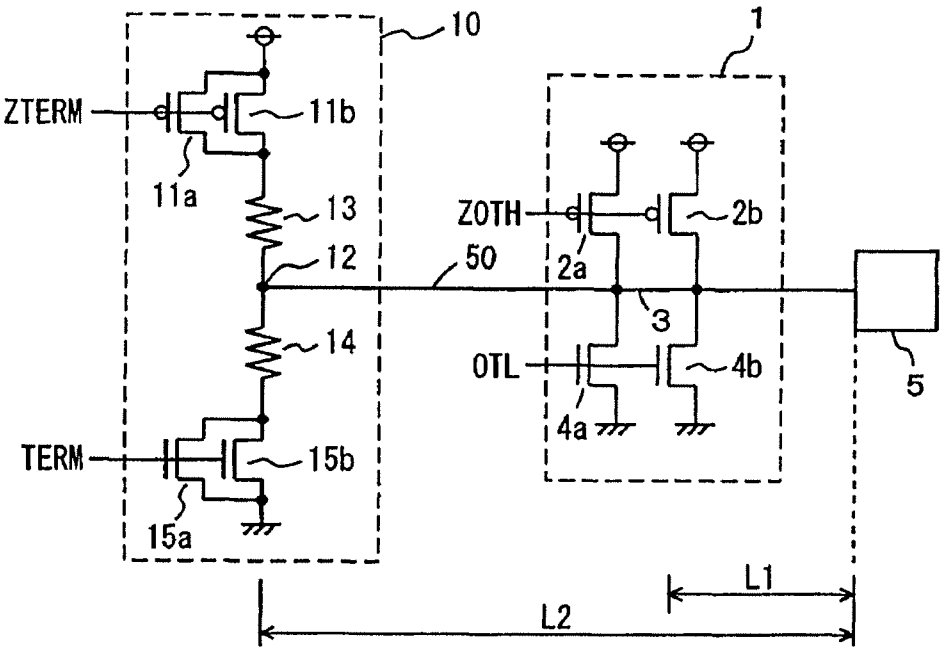
VSSQ
OTL

FIG.8

FIG.9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15b
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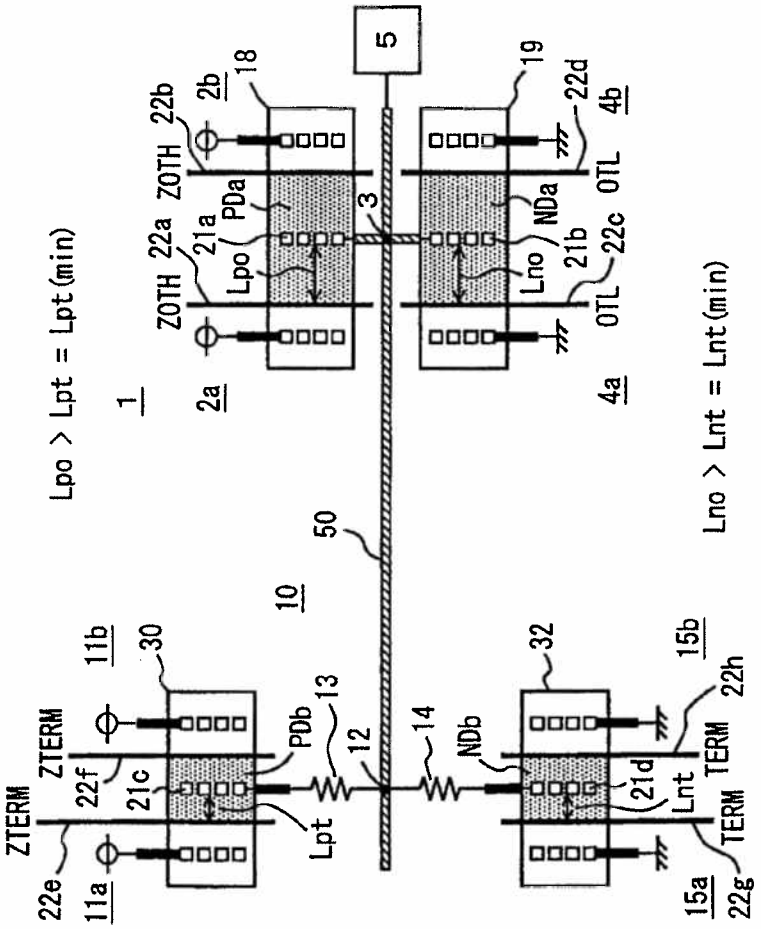
L1
L2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10
11a
11b
15a
15b
18
19
22a
22b
22c
22d
22e
22f
22g
22h
30
32
50
3
12
13
14
21a
21b
21c
21d
PDa
NDa
PDb
NDb
Lpo
Lno
Lpt
Lnt
ZOTH
OTL
ZTERM
TERM

FIG.10

FIG.11

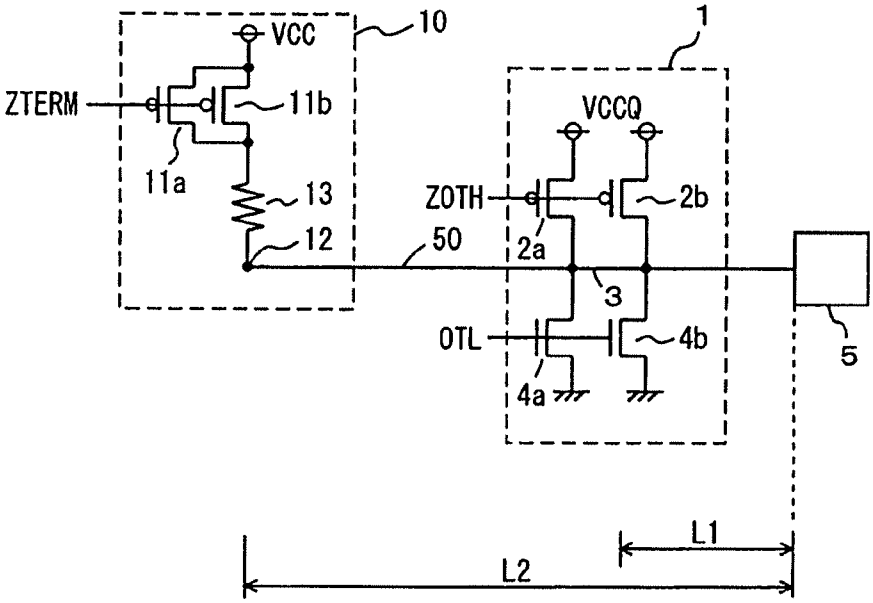


FIG.12

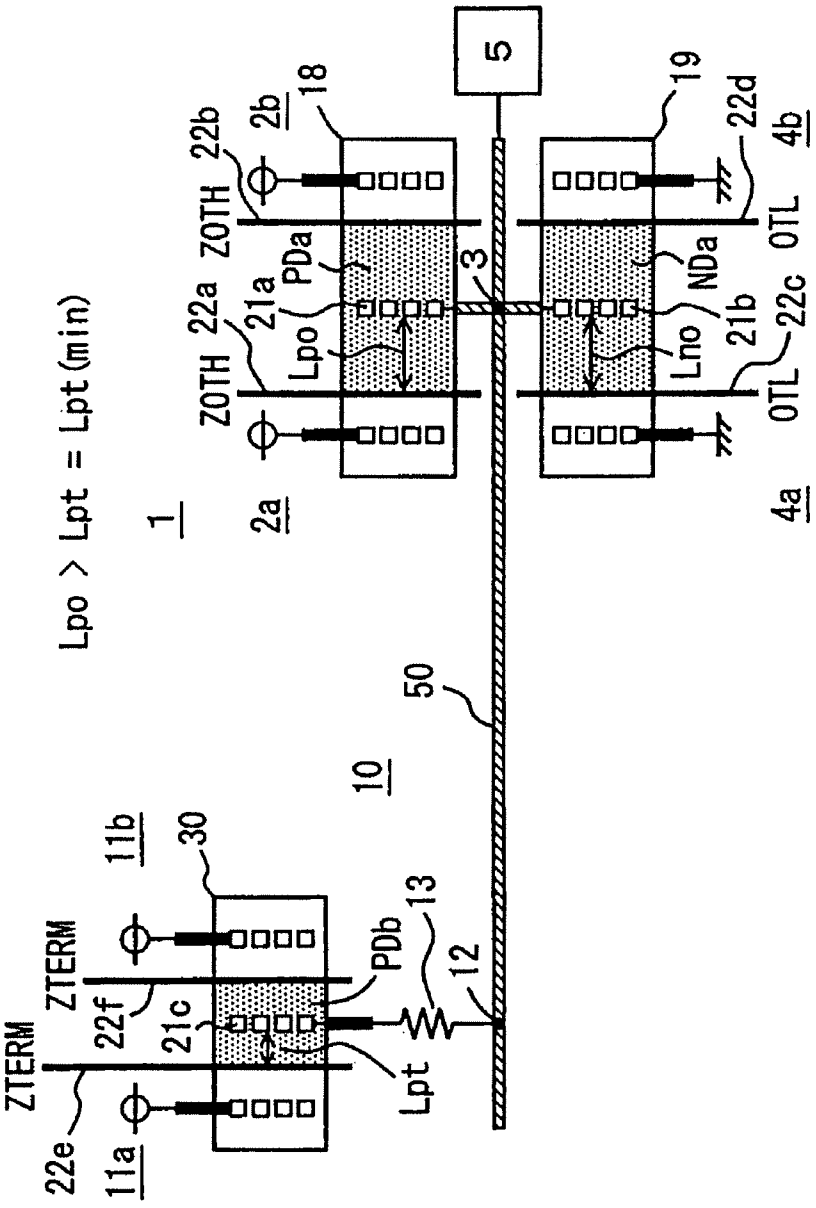

Lpo > Lpt = Lpt(min)
1
2a
2b
18
22b
ZOTH
22a
21a
PDa
Lpo
3
5
19
22d
4b
OTL
NDa
Lno
21b
22c
4a
50
10
11b
30
ZTERM
22f
21c
PDb
13
12
Lpt
22e
11a

FIG.13

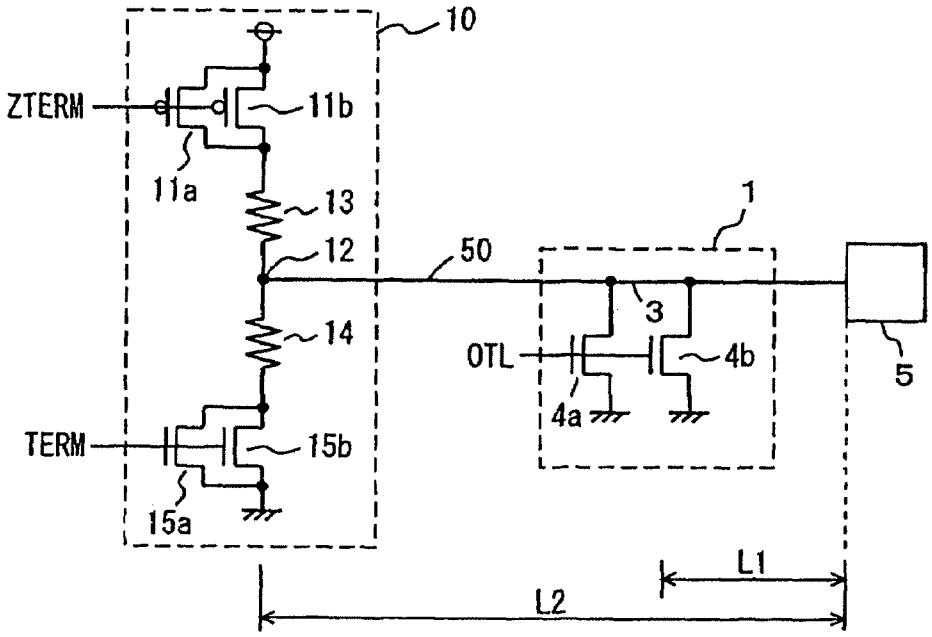


FIG.14

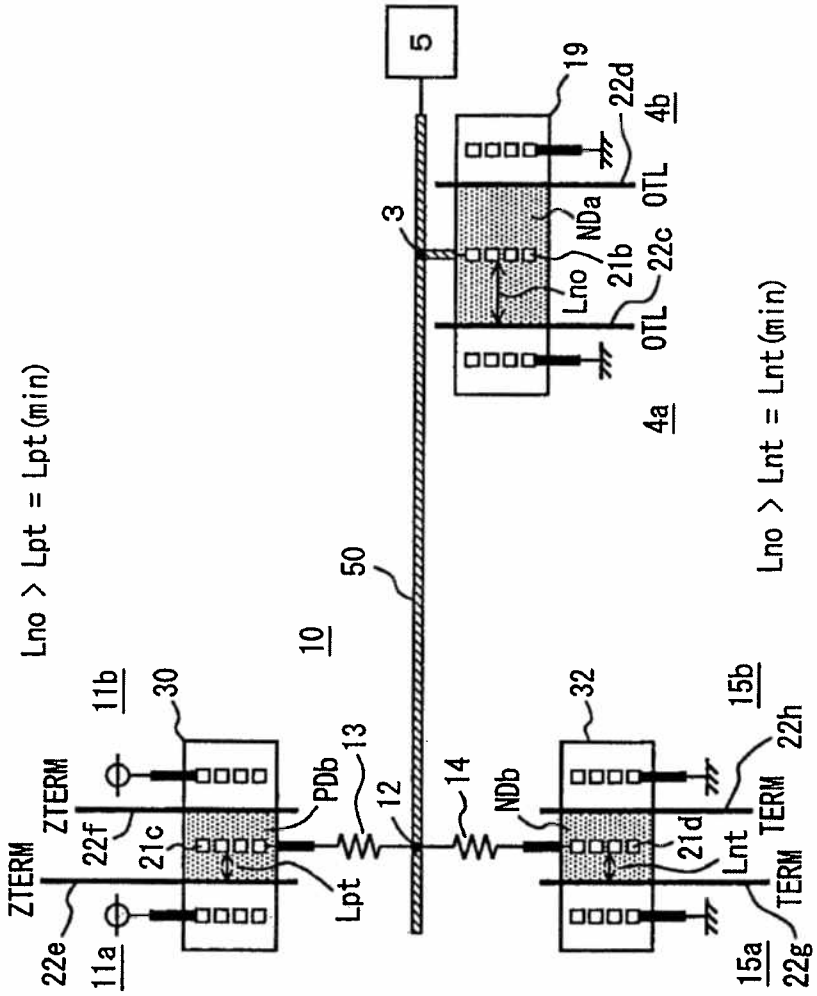

5
19
22d
4b
OTL
NDa
3
Lno
21b
22c
OTL
4a
Lno > Lnt = Lnt(min)
Lno > Lpt = Lpt(min)
50
10
11b
30
ZTERM
ZTERM
22f
21c
PDb
13
12
14
NDb
32
15b
22h
TERM
21d
Lnt
Lpt
22e
11a
15a
22g
TERM

FIG.15

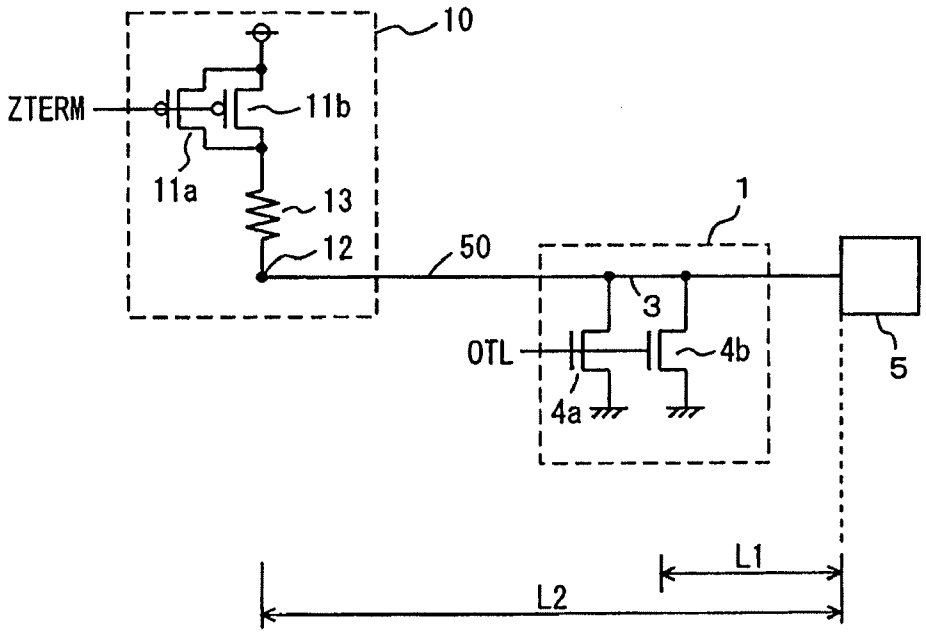


FIG.16

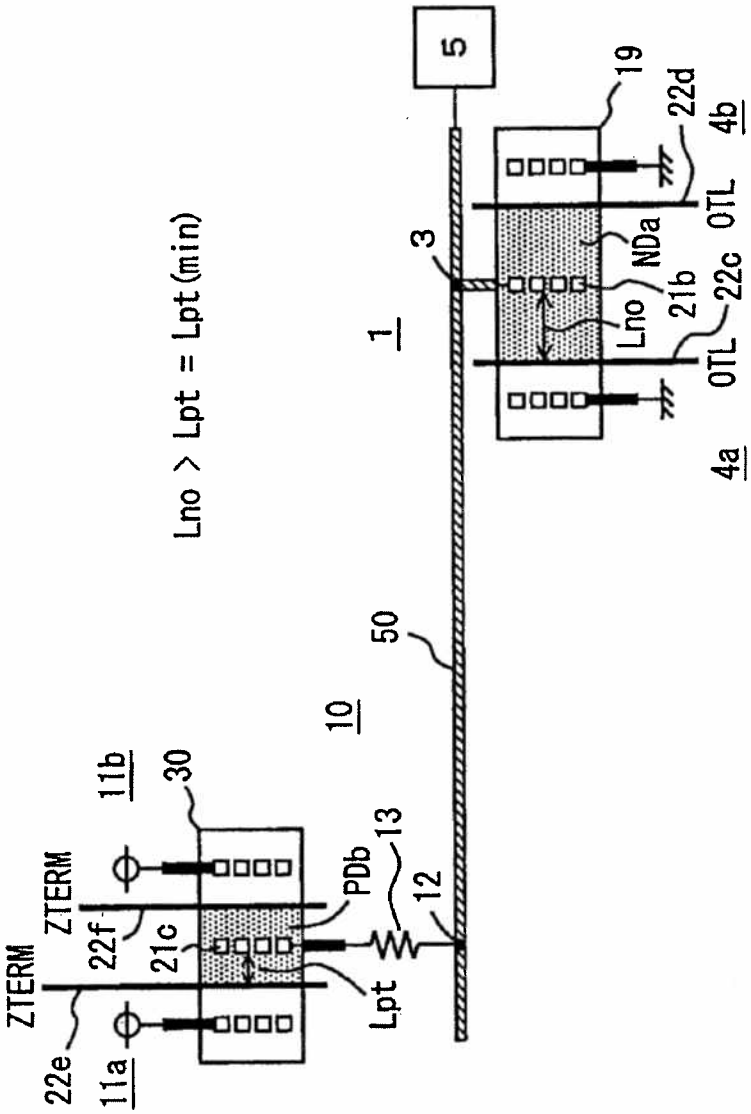
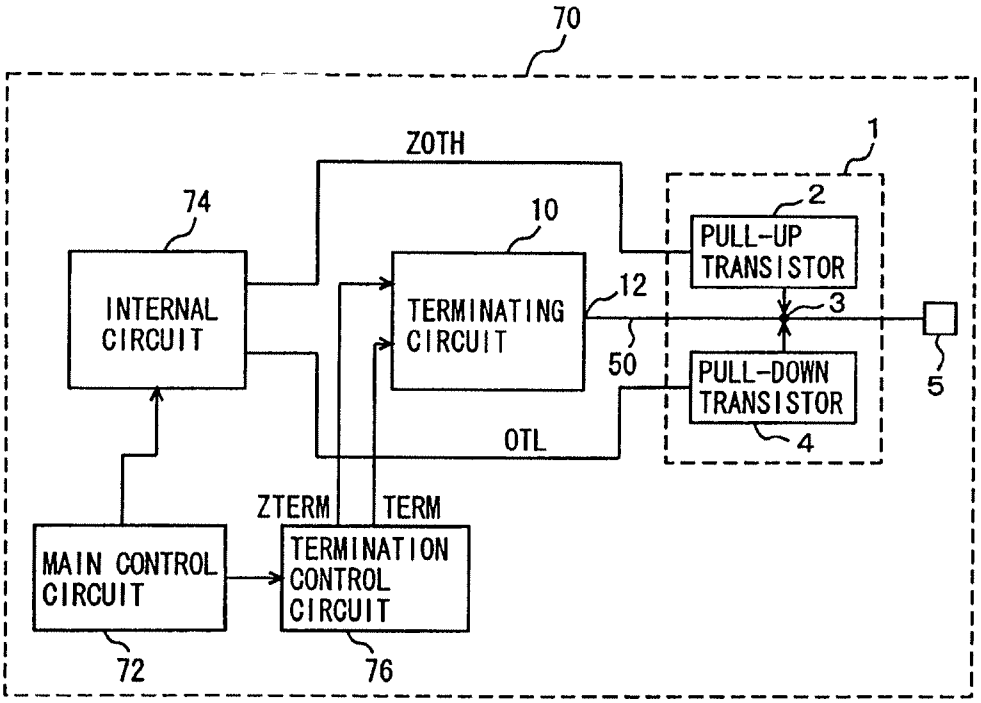

Lno > Lpt = Lpt(min)
5
19
22d
4b
OTL
NDa
3
22c
21b
Lno
1
OTL
4a
50
10
11b
30
13
PDb
12
ZTERM
ZTERM
22f
21c
Lpt
22e
11a

FIG.17


70
ZOTH
1
74
10
2
INTERNAL CIRCUIT
TERMINATING CIRCUIT
12
PULL-UP TRANSISTOR
3
50
PULL-DOWN TRANSISTOR
5
OTL
4
ZTERM
TERM
MAIN CONTROL CIRCUIT
TERMINATION CONTROL CIRCUIT
72
76

SEMICONDUCTOR DEVICE WITH BUS TERMINATING FUNCTION

RELATED APPLICATIONS

This application is a continuation of application Ser. No. 10/391,021 filed Mar. 19, 2003, which claims priority of Japanese Application No. 2002-307961, filed Oct. 23, 2002, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device driving an output node, and specifically, to a semiconductor device with a bus terminating function.

2. Description of the Background Art

In a semiconductor device, a transistor connected to a pin terminal is easy to be affected by noises, since it is directly connected to the outside of the device via the pin terminal. Among the noises, one at a level enough to destruct a device (a transistor) is referred to as a surge. A destruction of a semiconductor device by the surge is referred to as electrostatic damage (ESD), which is accompanied by breakdown of a gate insulating film of an MOS transistor (insulated gate field effect transistor) and others. Therefore, for the reliability of the semiconductor device, the breakdown voltage enough to withstand the surge is required.

For an input pin receiving an external signal, usually, an input protection circuit is configured by a diode or a diode-connected MOS transistor (insulated gate field effect transistor), or a field transistor with a sufficiently thick gate insulating film. By this input protection circuit, the surge is caused to flow to a power supply terminal or a ground terminal, and thus transmission of the surge to the internal circuitry is prevented.

The protection circuit is not required for an output circuit, since an output transistor serves as a surge absorbing transistor. However, in an MOS output circuit configured with an MOS transistor, a large current may flow into the output transistor or high electric field may be generated at drain due to the surge voltage, which may result in electrostatic damage. In order to reduce the current and the drain electric field for avoiding such electrostatic damage, the resistance value of drain region (hereinafter referred to as a drain diffusion resistance) in the output transistor must be increased. Usually, in order to increase the drain resistance, the distance between the gate of the output transistor and a drain contact for connecting to the output node is required to be sufficiently long. Consequently, the diffusion region area of the drain portion in the output transistor increases, and hence, the size of the output transistor increases.

An arrangement for preventing electrostatic damage with limited area of the output circuit is proposed in Japanese Patent Laying-Open No. 2001-127173. According to this first prior art document, drain diffusion region is made different in impurity concentration from source diffusion region, to have an increased drain diffusion resistance value.

In a second prior art document, Japanese Patent Laying-Open No. 11-214621, an arrangement is disclosed in which a terminating resistance element and a protection element for this terminating resistance element are provided between an output transistor and an output pad. According to this second prior art document, the electrostatic protection element is formed of an MOS transistor, and in order to increase the resistance of the drain region, i.e., drain diffusion resistance, the distance between gate and drain contact of the MOS transistor is made longer. Taking advantage of this large drain diffusion region area, the terminating resistance element is arranged above the drain region of the electrostatic protection element in order not to increase the layout area of the entire output circuit. The terminating resistance element is a current limiting resistance element for avoiding a reflecting wave such as a ringing in signal transmission, and is connected between the output pad and the output node (drain) of the output transistor.

In a third prior art document, Japanese Patent Laying-Open No. 10-65744, an arrangement is disclosed in which impedance switching means is provided between an output terminal and an output circuit. The impedance switching means is set to a low impedance state in transmission and to a high impedance state in reception, to reduce reflection noises due to capacitive load of transmission path.

According to the arrangement shown in the first prior art document, the impurity concentrations of source and drain in the output transistor must be made different, and hence, the number of manufacturing steps increases. The drain diffusion resistance is continuously connected to an external bus via the pin terminal. If the drain diffusion resistance functions as terminating resistance, then an output signal is driven via high drain diffusion resistance in signal outputting, and thus the signal can not be transmitted at high speed.

According to the arrangement disclosed in the second prior art document, the protection circuit for the terminating resistance element is arranged corresponding to the output circuit. The distance between a drain contact and a gate electrode of the MOS transistor of the protection circuit is large enough to place the terminating resistor thereabove. Accordingly, the interface area between the drain region and the substrate region is made large, and a large drain junction capacitance of this protection circuit is connected to the output pin terminal. Consequently, the parasitic capacitance of the output pin terminal increases, and thus, a signal can not be transmitted at high speed. Further, since the terminating resistance element is connected between the drain of the output transistor and the output pad and functions as a current limiting element for an output signal, the signal can not be output at high speed. Moreover, since the terminating resistance causes a voltage drop, a signal at CMOS level can not be transmitted.

According to the arrangement disclosed in the third prior art document, the impedance switching means is provided for the output pin terminal, which has the impedance switched between a transmission mode and a reception mode. In this case also, however, a protection element against the surge must be provided, which increases the occupying area of the circuit for switching the termination resistance value in accordance with the operation mode. Especially, if the circuit portion for controlling this termination resistance is formed with a transistor having an increased drain diffusion resistance, then the load of the output pin increases accordingly. Thus, a signal can not be transmitted at high speed, and the occupying area of the output circuit increases further. In the third prior art document, the consideration is only given to suppress the ringing in signal transmission and reception, and an arrangement for reducing the output circuit area and for alleviating the load of the transmission path is not considered.

Each of U.S. Pat. No. 6,809,546 B2 and US 2004/0032319 A1 discloses an on-chip termination circuit formed of series connection of a termination resistor and a MOS transistor, but fails to show the specific layout of the termination circuit as in the present application.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device capable of transferring a signal accurately at high speed, without increase in circuit area and degradation in reliability.

Another object of the present invention is to provide a semiconductor circuit device with an output circuit containing a terminating circuit, which is capable of transferring a signal of CMOS level at high speed with small occupying area and high reliability.

A semiconductor device according to the present invention includes a first output transistor driving an output node in accordance with an internal signal, a first resistance element having one end connected to the output node, and a first terminating transistor element connected between another end of the first resistance element and a first power supply node and selectively made conductive in accordance with an operation mode designating signal. The distance between a control electrode and a contact of one conduction terminal in the first terminating transistor is shorter than in the first output transistor.

By arranging the terminating circuit inside the semiconductor device, a signal can be transmitted through selective operation of the terminating circuit while maintaining the impedance matching to the bus, even when the system configuration is modified. Therefore, a signal can be transmitted at high speed with no adverse effect by an interconnection line impedance or others.

Additionally, by setting the drain contact-to-gate (control electrode) length in the terminating transistor shorter than in the output transistor, the area will not be increased despite of placing the terminating circuit. Further, by placing the terminating resistance element, the breakdown voltage against the surge of the terminating transistor can be assured. Thus, a reliable semiconductor device with a small occupying area, having an output circuit that is capable of transmitting a signal at high speed can be implemented.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the configuration of a semiconductor device according to a first embodiment of the present invention;

FIG. **2** schematically shows the two dimensional layout of the semiconductor device shown in FIG. **1**;

FIG. **3** schematically shows the two dimensional layout of a first modification of the first embodiment of the present invention;

FIG. **4** shows an electric equivalent circuit of the layout shown in FIG. **3**;

FIG. **5** schematically shows the two dimensional layout of a second modification of the first embodiment of the present invention;

FIG. **6** shows an electric equivalent circuit of the layout shown in FIG. **5**;

FIG. **7** schematically shows the two dimensional layout of a second modification of the first embodiment of the present invention;

FIG. **8** shows an electric equivalent circuit of the layout shown in FIG. **7**;

FIG. **9** shows the configuration of a semiconductor device according to a second embodiment of the present invention;

FIG. **10** schematically shows the two dimensional layout of the circuit shown in FIG. **9**;

FIG. **11** shows the configuration of a first modification of the second embodiment of the present invention;

FIG. **12** schematically shows the two dimensional layout of the circuit shown in FIG. **11**;

FIG. **13** shows the configuration of a second modification of the second embodiment of the present invention;

FIG. **14** schematically shows the two dimensional layout of the circuit shown in FIG. **13**;

FIG. **15** schematically shows the configuration of a third modification of the second embodiment of the present invention;

FIG. **16** schematically shows the two dimensional layout of the circuit shown in FIG. **15**; and

FIG. **17** schematically shows the overall configuration of a semiconductor device according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

FIG. **1** shows a configuration of a main part of a semiconductor device according to a first embodiment of the present invention. In FIG. **1**, an output circuit **1** and a terminating circuit **10** provided for an external output pad **5** are representatively shown. Pad **5** is connected to a pin terminal, which is not shown.

Output circuit **1** includes P-channel MOS transistors **2***a* and **2***b* each connected between a power supply node and an output node **3** and selectively made conductive in accordance with an output control signal ZOTH, and N-channel MOS transistors **4***a* and **4***b* each connected between output node **3** and a ground node and selectively made conductive in accordance with an output control signal OTL. Power supply voltage VCCQ for the output circuit is supplied to the power supply node, and ground voltage VSSQ for the output circuit is supplied to the ground node. Output node **3** is connected to output pad **5**.

The logic levels of output control signals ZOTH and OTL are set in accordance with an operating condition of output circuit **1** and an internal signal. When output control signal ZOTH is at H level (logical high level) and output control signal OTL is at L level (logical low level), MOS transistors **2***a*, **2***b*, **4***a* and **4***b* are all in an off state (non-conductive state), and output circuit **1** is set to an output high impedance state. In this output high impedance state, output circuit **1** is in standby state. When output control signals ZOTH and OTL are both at H level, MOS transistors **2***a* and **2***b* are both in off state while MOS transistors **4***a* and **4***b* are both in on state (conductive state), and output node **3** is driven to ground voltage VSSQ level.

When output control signals ZOTH and OTL are both at L level, MOS transistors **2***a* and **2***b* are both in on state while MOS transistors **4***a* and **4***b* are both in off state. Responsively, output node **3** is driven to power supply voltage for output circuit, or output power supply voltage VCCQ level.

In operation of output circuit **1**, output control signals ZOTH and OTL are generated in accordance with an internal signal. The internal signal is internal read data when the semiconductor device shown is applied to a memory device, and based on the internal data and a read operation timing control signal, these output control signals ZOTH and OTL are generated.

Two MOS transistors **2***a* and **2***b*, or two MOS transistors **4***a* and **4***b* are arranged in parallel for the following reasons.

These MOS transistors **2***a*, **2***b*, **4***a*, and **4***b* are each configured with unit MOS transistors, and using a plurality of unit transistors, required driving power is provided to output circuit **1**. Therefore, the number of pull-down N-channel MOS transistors for discharging the output and the number of pull-up P-channel transistors for charging the output are determined as appropriate in accordance with a power required for driving external pad **5** and the current drivability of the unit MOS transistor.

Terminating circuit **10** includes a resistance element **13** having one end connected to an output node **12**, P-channel MOS transistors **11***a* and **11***b* connected between another end of resistance element **13** and a power supply node and receiving a termination control signal ZTERM at their gates, a resistance element **14** having one end connected to an output node **12**, and N-channel MOS transistors **15***a* and **15***b* connected between the other end of resistance element **14** and a ground node and receiving a termination control signal TERM at their gates.

Voltages VCC and VSS applied to terminating circuit **10** are supplied from a power supply terminal different from that applying voltages VCCQ and VSSQ to output circuit **1**. By applying operation power supply voltages VCCQ and VSSQ dedicatedly to output circuit **1**, the operation of output circuit **1** can be stabilized, or the power supply noise in an output operation is prevented from being transmitted to other circuits. Voltages VCC and VSS applied to terminating circuit **10** may be supplied from the common power supply terminal that applies voltages VCCQ and VSSQ to output circuit **1**. Further, voltages VCC and VCCQ may be at the same voltage level, or may be at different voltage levels.

Termination control signals ZTERM and TERM are control signals complementary to each other. When activating the terminating operation of terminating circuit **10**, termination control signal ZTERM is set at L level and termination control signal TERM is set at H level. When deactivating the terminating operation of terminating circuit **10**, termination control signal ZTERM is set at H level and termination control signal TERM is set at L level.

As in output circuit **1**, in terminating circuit **10** as well, two MOS transistors **11***a* and **11***b* at H level side and two MOS transistors **15***a* and **15***b* at L level side are arranged, for forming these termination control P- and N-channel switching MOS transistors each with a plurality of unit MOS transistors.

In terminating circuit **10**, MOS transistors **11***a* and **11***b* are connected to output node **12** via resistance element **13**, while MOS transistors **15***a* and **15***b* are connected to output node **12** via resistance element **14**. Output node **12** is connected to output pad **5**. Therefore, MOS transistors **11***a*, **11***b*, **15***a*, and **15***b* for termination control are not necessarily required to comply with the drain contact-to-gate distance requirement that is specified to assure the reliability against electrostatic damage, and that is the requirement for output MOS transistors **2***a*, **2***b*, **4***a*, and **4***b* directly connected to the output pin. Accordingly, the drain contact-to-gate distances of MOS transistors **11***a* and **11***b* are set shorter than those of MOS transistors **2***a* and **2***b*, or the drain contact-to-gate distances of MOS transistors **15***a* and **15***b* are set shorter than those of MOS transistors **4***a* and **4***b*. By shortening the drain contact-to-gate distance, the drain resistance is reduced, and hence, the layout area of the drain region of each of terminating transistors **11***a*, **11***b*, **15***a*, and **15***b* is reduced.

The relationship between termination control signals TERM and ZTERM, and output control signals ZOTH and OTL for terminating circuit **10** are not specifically determined. The terminating operation of terminating circuit **10** may be activated in a signal/data output operation of output circuit **1**. Further, such an arrangement may be employed that the terminating operation of terminating circuit **10** is deactivated in a signal/data output operation of output circuit **1** and a terminating circuit of another circuit connected to a signal bus, not shown, is activated. Still further, where the pad **5** is further connected to a signal input pin and therefore to a not shown input circuit, the terminating operation of terminating circuit **10** may be deactivated or activated in a signal input operation.

The activation period of the terminating operation of terminating circuit **1** may be set in accordance with the condition of a load connected to an external bus.

Therefore, activation/deactivation timing and period of termination control signals TERM and ZTERM needs only to be determined as appropriate in accordance with the termination control condition of the bus of the system to which the semiconductor circuit device is applied.

FIG. **2** shows the two-dimensional layout of MOS transistors in output circuit **1** and terminating circuit **10** shown in FIG. **1**. In FIG. **2**, MOS transistors **2***a* and **2***b* of output circuit **1** are formed in a rectangular active region **18**, and output MOS transistors **4***a* and **4***b* are formed in a rectangular active region **19** arranged facing to active region **18**.

Active region **18** includes a drain impurity region PDa formed in the middle portion, and source impurity regions PSa and PSb formed at opposing sides thereof A gate electrode **22***a* is arranged between drain impurity region PDa and source impurity region PSa, and a gate electrode **22***b* is arranged between drain impurity region PDa and source impurity region PSb. Drain impurity region PDa is shared by transistors **2***a* and **2***b*. Output control signal ZOTH is commonly applied to these gate electrodes **22***a* and **22***b*.

Source impurity regions PSa and PSb are connected to power supply nodes via source contacts **20***a* and **20***b*, respectively. Drain impurity region PDa is connected to output node **3** via drain contact **21***a*. The distance between drain contact **21***a* and gate electrode **22***a* is Lpo. Similarly, although not shown explicitly, the distance between drain contact **21***a* and gate electrode **22***b* of MOS transistor **2***b* is also Lpo.

In active region **19** also, an N-type drain impurity region NDa is arranged in the middle portion, and at opposing sides thereof, N-type source impurity regions NSa and NSb are arranged. A gate electrode **22***c* is arranged between N-type source impurity region NSa and N-type drain impurity region NDa, and a gate electrode **22***d* is arranged between drain impurity region NDa and source impurity region NSb. Drain impurity region NDa is shared by MOS transistors **4***a* and **4***b*. Drain impurity region NDa is connected to output node **3** via drain contact **21***b*. The distance between drain contact **21***b* and gate electrode **22***c* is Lno. Similarly, though not shown explicitly in FIG. **2**, the distance between drain contact **21***b* and gate electrode **22***b* is also Lno. Source impurity regions NSa and NSb are electrically connected to ground nodes via source contacts **22***c* and **22***d*, respectively.

In terminating circuit **10**, terminating MOS transistors **11***a* and **11***b* are formed in P-type active region **30**, while MOS transistors **15***a* and **15***b* are formed in N-type active region **32**. In P-type active region **30**, a drain impurity region PDb is formed in the middle portion, and at opposing sides thereof, source impurity regions PSc and PSd are formed. A gate electrode **22***e* is provided between drain impurity region PDb and source impurity region PSc, and gate electrode **22***f* is arranged between drain impurity region PDb and source impurity region PSd.

Impurity region PDb is shared by MOS transistors **11***a* and **11***b*. Drain impurity region PDb is connected to the other end of resistance element **13** via drain contact **21***c*. Source impurity regions PSc and PSd are electrically connected to power supply nodes via source contacts **20***e* and **20***f*, respectively. The distance between drain contact **21***c* and gate electrode **22***e* is Lpt, and the distance between drain contact **21***c* and gate electrode **22***f* is also Lpt. In FIG. **2**, drain contact-to-gate distance of MOS transistor **11***a* is indicated.

In N-type active region **32**, an N-type drain impurity region NDb is formed at the middle portion, and at opposing sides thereof, N-type source impurity regions NSc and NSd are arranged. A gate electrode **22***g* is arranged between N-type source impurity region NSc and N-type drain impurity region NDb, and a gate electrode **22***h* is arranged between N-type drain impurity region NDb and N-type source impurity region NSd. Source impurity regions NSc and NSd are electrically connected to ground nodes via source contacts **20***g* and **20***h*, respectively. Drain impurity region NDb is connected to the other end of resistance element **14** via drain contact **21***d*. Resistance elements **13** and **14** each have the one end connected to node **12**. The distance from drain contact **21***d* to gate electrodes **22***g* and to **22***h* of MOS transistor **15***a* and **15***b*, respectively, is Lnt.

The drain contact-to-gate electrode distance Lpo of MOS transistors **2***a* and **2***b* is longer than the drain contact-to-gate electrode distance Lpt of MOS transistors **11***a* and **11***b*. The drain contact-to-gate electrode distance Lno of MOS transistors **4***a* and **4***b* is longer than the drain contact-to-gate electrode distance Lnt of MOS transistors **15***a* and **15***b*.

If drain impurity regions PDa and PDb are the same in impurity concentration, and if drain impurity regions NDa and NDb are the same in impurity concentration, then shorter drain contact-to-gate electrode distance results in smaller drain resistance. In this case, the electric field relaxation by resistance elements **13** and **14** can compensate for the reduction of drain resistance of MOS transistors **11***a*, **11***b*, **15***a* and **15***b* in terminating circuit **10**.

Terminating resistance elements **13** and **14** may be configured with diffusion resistance, or may be configured with polysilicon resistance.

As shown in FIG. **2**, the length of P-type active region **30** in horizontal direction in FIG. **2** is shorter than P-type active region **18** by at least 2·(Lpo−Lpt). Similarly, the length of N-type active region **32** in horizontal direction is shorter than N-type active region **19** by at least 2·(Lno−Lnt). Therefore, in terminating circuit **10**, the occupying area of active regions **30** and **32** can be reduced, as compared to the case of the countermeasure against the electrostatic damage similar to that for MOS transistor **2***a*, **2***b*, **4***a*, and **4***b* in output circuit **1**. Accordingly, the occupying area of terminating circuit **10** can be reduced, and thus to suppress the increase in occupying area of the semiconductor circuit device including this output circuit and terminating circuit **10**. The relaxation of electric field/current at drain in terminating transistor **11***a*, **11***b*, and **15***a*, **15***b* is achieved by resistance elements **13** and **14**, respectively, and thus the electrostatic damage of terminating transistors **11***a*, **11***b*, **15***a*, and **15***b* can be prevented.

Further, by using terminating circuit **10**, a signal can be transmitted at high speed via pad **5**, while maintaining impedance matching with the bus.

In the arrangement shown in FIG. **2**, the drain contact-to-gate electrode distance satisfies the following relation:

Lpo>Lpt, Lno>Lnt

However, the following conditional relation may be satisfied as well:

Lpo>Lpt, Lno>Lpt,

Lpo>Lnt, and Lno>Lnt.

In the arrangement shown in FIG. **2**, with output transistors **2***a*, **2***b*, **4***a*, and **4***b* each comprised of a unit transistor, the output circuit **1** is constructed, and similarly in terminating circuit **10**, MOS transistors **11***a*, **11***b*, **15***a*, and **15***b* each comprised of a unit transistor are employed for constructing pull-up and pull-down terminating transistors. However, in accordance with the load of pad **5**, the output control transistor or the termination control transistor may be formed using three or more unit transistors. Increasing the numbers of unit transistors employed, the effect of area saving achieved by the decreased drain contact-to-gate electrode distance will be more significant.

First Modification

FIG. **3** schematically shows a layout of transistors in output circuit **1** and terminating circuit **10** according to a first modification of the first embodiment of the present invention. The layout of the semiconductor circuit device shown in FIG. **3** is different from that of FIG. **2** in the following points. No pulling-down termination circuit portion is provided in terminating circuit **10**. Terminating resistance element **13** and P-type active region **30** forming P-channel MOS transistors **11***a* and **11***b* are provided. In P-type active region **30**, the distances Lpt from drain contact **21***c* to gate electrode **22***e* and to gate electrode **22***f*, respectively, are set sufficiently shorter as compared with the corresponding distance Lpo of P-channel MOS transistors included in output circuit **1**. In this case, the distance Lpt is set shorter than the drain contact-to-gate electrode distance Lno of N-channel MOS transistors of output circuit **1**.

The other configuration of the circuit layout shown in FIG. **3** is the same as that shown in FIG. **2**, therefore corresponding parts are denoted by identical reference numerals or characters and detailed description thereof will not be repeated.

In the arrangement shown in FIG. **3**, the configuration of output circuit **1** is identical to the configuration shown in FIG. **2**. In terminating circuit **10**, since pulling-down resistance element and N-channel MOS transistors are not provided, the occupying area of terminating circuit **10** as well as the parasitic capacitance associated with node **12** can be decreased, allowing output circuit **1** to drive pad **5** at high speed.

FIG. **4** shows an electric equivalent circuit of the configuration shown in FIG. **3**. As shown in FIG. **4**, in terminating circuit **10**, resistance element **13** has one end connected to node **12**, and between this resistance element **13** and power supply node, P-channel MOS transistors **11***a* and **11***b* receiving termination control signal ZTERM at their gates are connected.

Output circuit **1** includes, similarly to the configuration shown in FIG. **1**, pulling-up transistors **2***a* and **2***b*, and pulling-down transistors **4***a* and **4***b*.

Terminating circuit **10** can perform the terminating operation at high speed on node **12** with reduced parasitic capacitance, owing to the small drain diffusion resistance of MOS transistors **11***a* and **11***b* and absence of pull-down transistors **15***a* and **15***b*. The terminating operation condition is the same as described above referring to FIG. **1** and determined as appropriate in accordance with the bus termination condition of the system involved.

Further, in terminating circuit **10**, since drain junction capacitances of MOS transistors **15***a* and **15***b* shown in FIG. **1** will not be coupled to pad **5** via resistance element **13**, the load of pad **5** can be reduced, allowing output circuit **1** to drive the pad **5** at high speed.

The configuration of output circuit **1** is the same as the configuration of output circuit **1** shown in FIG. **1**, and pad **5** is driven via output node **3** in accordance with output signals ZOTH and OTL.

In termination control circuit **10** shown in FIG. **3**, in pulling-down operation, pad **5** is pulled up to power supply voltage VCC level. The termination voltage VCC may be the same voltage as voltage VCCQ of output circuit **1**, or may be applied from a different power supply terminal. Further, the voltages VCC and VCCQ may be at the same voltage level or may be at different voltage levels. Terminating circuit **10** may be configured only with a pulling-down circuit that drives the pad **5** to ground voltage level in the terminating operation (i.e., may be configured with resistance element **14** and MOS transistors **15***a* and **15***b*).

Second Modification

FIG. **5** schematically shows the layout of an output circuit and a terminating circuit according to a second modification of the first embodiment of the present invention. The layout shown in FIG. **5** is different from the layout shown in FIG. **2** in the following points. P-type active region **18** is not arranged, but an N-type active region **19** is arranged in output circuit **1**. The distance between drain contact **21***b* and gate electrode **22***c* in N-type active region **19** is set to Lno. Source impurity regions NSa and NSb are coupled to ground nodes via source contacts **20***c* and **20***d*, respectively.

In output circuit **1**, MOS transistors **4***a* and **4***b* are arranged to drive output node **3** in accordance with output control signal OTL applied to gate electrodes **22***c* and **22***d*. Accordingly, the output circuit **1** drives the external signal line via output pad **5**, according to the open-drain scheme.

The configuration of terminating circuit **10** is similar to the layout of terminating circuit **10** shown in FIG. **2**, therefore identical reference numerals or characters are allotted to corresponding parts, and detailed description thereof will not be repeated.

In the configuration shown in FIG. **5**, the drain contact-to-gate electrode distances Lpt of P-channel MOS transistors **11***a* and **11***b* included in terminating circuit **10** are set shorter than the gate electrode-to-drain contact distances Lno of N-channel MOS transistors **4***a* and **4***b* included in output circuit **1**. Similarly, drain contact-to-gate electrode distances Lnt of N-channel MOS transistors **15***a* and **15***b* are set shorter than the drain contact-to-gate electrode distances Lno of N-channel MOS transistors **4***a* and **4***b* included in output circuit **1**.

This output circuit **1** includes only the circuit of open-drain scheme, which pulls down output node **3** in accordance with output control signal OTL. To output node **3**, only the pulling-down N-channel MOS transistors are connected, thus the load of output node **3** is reduced and the pad **5** can be driven at high speed.

FIG. **6** shows an electric equivalent circuit of the configuration shown in FIG. **5**. Referring to FIG. **6**, in output circuit **1**, N-channel MOS transistors **4***a* and **4***b* receiving output control signal OTL at their gates are arranged in parallel between output node **3** and ground nodes. The circuit configuration of the terminating circuit **10** is the same as terminating circuit **10** shown in FIG. **1**. Terminating transistors **11***a*, **11***b*, **15***a* and **15***b*, as well as terminating resistors **13** and **14** are provided.

After output pad **5** is driven to ground voltage VSSQ level by output circuit **1** in accordance with output control signal OTL, the pad **5** can be precharged to power supply voltage VCC level again, using terminating circuit **10**. Additionally, since the output circuit of open-drain scheme is employed, the load of output circuit **1** is reduced, and thus an output signal can be generated at high speed.

In the configuration of open-drain scheme output circuit **1** also, in terminating circuit **10**, the gate electrode-to-drain contact distance of each of the MOS transistors included therein is set short and thus the occupying area of terminating circuit **10** is sufficiently small. Therefore, an output signal can be generated at high speed accurately while suppressing the increase in circuit occupying area.

Third Modification

FIG. **7** schematically shows a layout of a third modification of the semiconductor device according to the first embodiment of the present invention. The layout of the semiconductor device shown in FIG. **7** is different from the layout of the semiconductor device shown in FIG. **5** in the following points. Resistance element **14** and N-type active region **32** are not provided in terminating circuit **10** and resistance element **13** and P-type active region **30** are provided. Specifically, P-channel MOS transistors **11***a* and **11***b* terminating at power supply voltage level are provided in terminating circuit **10**. The distances Lpt from drain contact **21***c* to gate electrodes **22***e* and **22***f* of P-channel MOS transistors **11***a* and **11***b*, respectively, are set shorter than the drain contact-to-gate electrode distances Lno of N-channel MOS transistors included in output circuit **1**. Source impurity regions PSc and PSd are connected to power supply nodes via source contacts **20***e* and **20***f*, respectively.

Similarly, in output circuit **1**, source impurity regions NSa and NSb in N active region **19** are connected to ground nodes via source contacts **20***c* and **20***d*, respectively. Specifically, in output circuit **1**, similarly to the configuration shown in FIG. **5**, N-channel MOS transistors **4***a* and **4***b* are provided, but pulling-up P-channel MOS transistors are not provided.

In the configuration shown in FIG. **7**, pad **5** is driven to ground voltage level by N-channel MOS transistors **4***a* and **4***b* in accordance with open-drain scheme, and pad **5** is terminated at power supply voltage level.

In the configuration of terminating circuit **10** and output circuit **1** shown in FIG. **7**, output pad **5** is driven in open-drain scheme, and terminating circuit **10** terminates output pad **5** to power supply node at appropriate timing in accordance with the bus condition. The loads on output pad **5** are only the drain junction capacitances and the interconnection line capacitances of active regions **19** and **30**, and the drain junction capacitances of N-channel MOS transistors in terminating circuit **10** are eliminated, and thus, output pad **5** is driven at higher speed.

FIG. **8** shows an electric equivalent circuit of the semiconductor device shown in FIG. **7**. Referring to FIG. **8**, in terminating circuit **10**, there are arranged resistance element **13**, and P-channel MOS transistors **11***a* and **11***b* that selectively connect resistance element **13** to power supply node in accordance with termination control signal ZTERM.

In output circuit **1**, N-channel MOS transistors **4***a* and **4***b* are connected in parallel, which drive output node **3** to ground voltage VSSQ level in accordance with output control signal OTL. Therefore, by driving output pad **5** in the open-drain scheme and by terminating the pad **5** at power supply voltage VCC level, the load of pad **5** is reduced and a signal can be transmitted at high speed. Power supply voltage VCC applied to terminating circuit **10** may be power supply voltage VCCQ, or may be a different voltage.

In this case also, the drain contact-to-gate electrode distance Lpt of each of terminating P-channel MOS transistors **11***a* and **11***b* is set sufficiently shorter than the drain contact-to-gate electrode distance Lno of each of N-channel MOS

transistors **4***a* and **4***b* of output circuit **1**, whereby the occupying area of terminating circuit **10** is made sufficiently small.

In general, an output pad is driven to ground voltage VSSQ level in the open-drain scheme. Alternatively, a pulling-up transistor for performing a pulling up to power supply voltage level in accordance with an output control signal may be provided in output circuit **1**, while a transistor performing a termination at ground voltage level may be provided in terminating circuit **10**.

Where both of a P-channel MOS transistor and an N-channel MOS transistor are used in output circuit **1**, the drain contact-to-gate electrode distance Lpo of P-channel transistor and the drain contact-to-gate electrode distance Lno of N-channel transistor may not be made equal to each other. Additionally, where both of a P-channel MOS transistor and a N-channel MOS transistor are used in terminating circuit **10**, the drain contact-to-gate electrode distance Lpt and the drain contact-to-gate electrode distance Lnt thereof may not be equal to each other.

The minimum requirement is that the drain contact-to-gate electrode distance of the MOS transistor in the terminating circuit is shorter than the drain contact-to-gate electrode distance of the MOS transistor in the output circuit, and the layout area of such terminating MOS transistors is sufficiently smaller than that of output MOS transistors.

As above, according to the first embodiment of the present invention, the drain contact-to-gate electrode distances of terminating MOS transistors are set shorter than those of output MOS transistors. Accordingly, the layout area of terminating circuit can be reduced sufficiently as compared to a configuration with conventional protection mechanism against electrostatic damage, and thus the occupying area of signal output portion can be reduced.

Further, since the terminating circuit is provided in a semiconductor device, the bus termination condition can be optimized in accordance with the bus utilization condition, and thus a signal/data can be transmitted accurately at high speed, while maintaining bus impedance matching.

Second Embodiment

FIG. **9** schematically shows a configuration of an output circuit and a terminating circuit according to a second embodiment of the present invention (hereinafter, both of the circuits are collectively referred to as a semiconductor device). In the configuration shown in FIG. **9**, output node **3** of output circuit **1** is electrically connected to pad **5** via interconnection line **50**. Terminating circuit **10** is provided distant from pad **5** relative to output circuit **1**. A terminating node **12** of terminating circuit **10** is connected to the same interconnection line **50**. Terminating node **12** of terminating circuit **10** and output node **3** of output circuit **1** are electrically connected to pad **5** via common interconnection line **50**.

Similarly to the first embodiment, output circuit **1** includes pulling up P-channel MOS transistors **2***a* and **2***b*, and pulling down N-channel MOS transistors **4***a* and **4***b*, which drive output node **3** in accordance with output control signals ZOTH and OTL, respectively.

Similarly to the first embodiment, terminating circuit **10** includes, as its components, resistance elements **13** and **14**, P-channel MOS transistors **11***a* and **11***b* that are selectively made conductive in accordance with termination control signal ZTERM, and N-channel MOS transistors **15***a* and **15***b* that are selectively made conductive in accordance with termination control signal TERM.

The operations of terminating circuit **10** and output circuit **1** are the same as in the first embodiment, and the logic level of termination control signals ZTERM and TERM for terminating circuit **10** is set in accordance with the termination condition of an external bus connected to pad **5** and the operation of output circuit **1**.

In the configuration shown in FIG. **9**, termination node **12** of terminating circuit **10** and output node **3** of output circuit **1** are connected to pad **5** via common interconnection line **50**. This interconnection line **50** extends from pad **5** to terminating circuit **10** via output circuit **1**. Therefore, a distance L2 between termination node **12** of terminating circuit **10** and pad **5** is made longer than a distance L1 between output node **3** of output circuit **1** and pad **5**.

In operation, output circuit **1** and terminating circuit **10** drive the pad **5** via common interconnection line **50**. In output circuit **1**, input capacitance to pad **5** exists due to the interconnection line and junction capacitances of MOS transistors **2***a*, **2***b*, **4***a* and **4***b*. Additionally, there exists a line resistance in interconnection line **50**. Accordingly, a low pass filter is formed by the parasitic capacitance and the interconnection line resistance in a path from pad **5** to terminating circuit **10** via interconnection line **50**. Even though a surge is generated at pad **5**, the steep surge is mitigated by the parasitic low pass filter and then transmitted to terminating circuit **10**.

In output circuit **1**, MOS transistors **2***a*, **2***b*, **4***a*, and **4***b* each have the drain contact-to-gate electrode distance set sufficiently long to have large drain resistance, and therefore the reliability against surge is assured. In terminating circuit **10**, the surge is mitigated by the parasitic low pass filter formed by output circuit **1** and interconnection line **50**, and then transmitted. Therefore, in terminating circuit **10**, the requirement of assuring reliability against the surge for MOS transistors **11***a*, **11***b*, **15***a*, and **15***b* is further relaxed. When the surge is sufficiently mitigated by resistance elements **13** and **14** and the parasitic low pass filter, the drain contact-to-gate electrode distances of MOS transistors **11***a*, **11***b*, **15***a*, and **15***b* in terminating circuit **10** can be shortened down to the limitation in designing, i.e., to the minimum design size, and thus the occupying area of terminating circuit **10** can be reduced.

FIG. **10** schematically shows a configuration of layout of the semiconductor device shown in FIG. **9**. In FIG. **10**, output circuit **1** is arranged proximate to pad **5**, and terminating circuit **10** is arranged far away from pad **5** as compared to output circuit **1**. Termination node **12** of terminating circuit **10** and output node **3** of output circuit **1** are connected to pad **5** by common interconnection line **50**.

Output circuit **1** includes P-type active region **18** for forming P-channel MOS transistors, and N-type active region **19** for forming N-channel MOS transistors, as in the first embodiment. In output circuit **1**, a part that correspond to a component of output circuit **1** of the first embodiment shown in FIG. **2** is allotted an identical reference numeral or character, and detailed description thereof will not be repeated.

In P-type active region **18**, the distances from drain contact **21***a*, formed in drain impurity region PDa, to gate electrode **22***a* and to gate electrode **22***b* each are Lpo. In N-type active region **19**, the distances from drain contact **21***b*, formed in drain impurity region NDa, to gate electrode **22***c* and to gate electrode **22***d* each is Lpo. In FIG. **10**, only one of the drain contact-to-gate distance for each active region is indicated. By setting the distances Lpo and Lno longer, the drain resistance is increased and the reliability against the surge generated at pad **5** can be assured.

The layout of terminating circuit **10** is identical to that of terminating circuit **10** shown in FIG. **2**, except that it is arranged further away from pad **5** via interconnection line **50** as compared to output circuit **1**. As for this terminating circuit **10**, corresponding parts are allotted with identical reference numerals or characters, and detailed description thereof will not be repeated.

In P-type active region **30**, the distances from drain contact **21***c*, formed in drain impurity region PDb, to gate electrodes **22***e* and **22***f* of MOS transistors **11***a* and **11***b* each are Lpt. In N-type active region **32**, the distances between drain contact **21***d*, formed in drain impurity region NDb, and gate electrodes **22***g* and **22***h* of MOS transistors **15***a* and **15***b*, respectively, are each Lnt. As previously described, since termination node **12** is electrically connected to pad **5** via interconnection line **50** and output node **3**, a parasitic low pass filter is connected equivalently to this termination node **12**. Accordingly, the drain contact-to-gate electrode distances Lpt and Lnt are set to minimum design size of Lpt (min) and Lnt (min) on designing, respectively. Thus, the layout area of active regions **30** and **32** can be reduced, and hence the occupying area of terminating circuit **10** can further be reduced.

It should be noted that in the second embodiment also, it is not necessary to set Lpt and Lnt equal to each other, nor Lpo and Lno equal to each other.

First Modification

FIG. **11** shows a configuration of a first modification of the second embodiment of the present invention. In a semiconductor device shown in FIG. **11**, terminating circuit **10** terminates the pad **5** at power supply voltage VCC. This termination voltage VCC is applied from a power supply terminal different from the terminal that applies power supply voltage VCCQ to output circuit **1**. These voltages VCCQ and VCC may be at the same voltage level, or may be at different voltage levels.

Terminating circuit **10** includes resistance element **13** having one end connected to termination node **12**, and P-channel MOS transistors **11***a* and **11***b* connecting the other end of resistance element **13** to a power supply node in accordance with termination control signal ZTERM.

In terminating circuit **10**, no transistor terminating at ground is provided. The configuration of output circuit **1** is identical to that of output circuit **1** shown in FIG. **9**, thus corresponding parts are allotted with identical reference numerals or characters, and detailed description thereof will not be repeated.

In the configuration shown in FIG. **11** also, termination node **12** of terminating circuit **10** is connected to pad **5** via output node **3** of output circuit **1** by interconnection line **50**. Accordingly, the distance L2 from termination node **12** of terminating circuit **10** to pad **5** is sufficiently longer than the distance L1 between output node **3** of output circuit **1** and pad **5**, similarly to the configuration shown in FIG. **9**. In this interconnection line **50**, the parasitic resistance and the parasitic capacitance thereof mitigate the surge abruptly inputted to the output pad **5**, and additionally, terminating resistor **13** mitigates the surge voltage, and thus the steep voltage by the surge is changed to a moderate voltage. Accordingly, the drain contact-to-gate electrode distance of MOS transistors **11***a* and **11***b* in terminating circuit **10** is set sufficiently shorter than that of MOS transistors **2***a* and **2***b* in output circuit **1**, and thus the drain resistances of the terminating MOS transistors are reduced.

FIG. **12** schematically shows the layout of the semiconductor device shown in FIG. **11**. The layout of the semiconductor device shown in FIG. **12** is identical to that of FIG. **10**, except that resistance element **14** and N-type active region **32** is removed from terminating circuit **10**. Accordingly, in the configuration shown in FIG. **12**, the parts corresponding to the components shown in FIG. **10** are allotted with identical reference numerals or characters and detailed description thereof will not be repeated.

In this arrangement where terminating circuit **10** terminates by power supply, the drain contact-to-gate electrode distance Lpt is set sufficiently shorter than the drain contact-to-gate electrode distance Lpo of each of MOS transistors **2***a* and **2***b* of output circuit **1**, and preferably, the distance Lpt is set to minimum design size Lpt (min). In this case, the distance Lpt is also set shorter than the drain contact-to-gate electrode distance Lno of each discharging MOS transistor in output circuit **1**.

Accordingly, also in this the configuration where terminating circuit **10** terminates at power supply voltage VCC, interconnection line **50** has input capacitance of output circuit **1** as well as interconnection line capacitance and interconnection line resistance, and thus a low pass filter is formed, which mitigates the surge for transmission to terminating circuit **10**. Even though the drain contact-to-gate electrode distance in terminating circuit **10** is set to minimum design size Lpt (min), since the surge is sufficiently mitigated and then transmitted, the reliability of these transistors **11***a* and **11***b* on occurrence of the surge can be sufficiently maintained.

Accordingly, the effect similar to that provided by the configurations shown in FIGS. **9** and **10** can be provided. Further, since terminating circuit **10** only terminates at power supply voltage VCC level and does not terminate at ground level, the occupying area of terminating circuit **10** can further be decreased. Terminating voltage VCC of terminating circuit **10** may be at an identical voltage level to power supply voltage VCCQ or may be at a different voltage level.

Second Modification

FIG. **13** shows a configuration of a second modification of the semiconductor device according to the second embodiment of the present invention. In the semiconductor device shown in FIG. **13**, an output circuit of open-drain scheme that drives output node **3** to ground voltage level is employed as output circuit **1**. Specifically, N-channel MOS transistors **4***a* and **4***b* that drives output node **3** to ground voltage level in accordance with output control signal OTL are provided in output circuit **1**. No pulling up P-channel MOS transistors are provided in output circuit **1**.

The configuration of terminating circuit **10** is identical to that of terminating circuit **10** shown in FIG. **9**, therefore corresponding parts are allotted with identical reference numerals or characters, and detailed description thereof will not be repeated. Termination node **12** of this terminating circuit **10** is connected to pad **5** via output node **3** of output circuit **1** by interconnection line **50**. The distance between termination node **12** and pad **5** is L2, while the distance between output node **3** and pad **5** is L1. Even though the surge is generated at pad **5**, since transmission of the surge to terminating circuit **10** is made via interconnection line **50**, the surge can be sufficiently mitigated and then transmitted to terminating circuit **10**.

Accordingly, when output circuit **1** is an output circuit of open-drain scheme also, the input capacitance due to the drain junction capacitances of MOS transistors **4***a* and **4***b* and the parasitic capacitance of interconnection line **50** as well as the parasitic resistance of interconnection line **50** exists. Therefore, since a low pass filter is parasitically connected to termination node **12**, the protection against the

surge is established. Thus, these four MOS transistors **11***a*, **11***b*, **15***a*, and **15***b* do not require specific countermeasure against surge and their drain-to-gate electrode distances can be reduced, and the layout area of terminating circuit **10** can be reduced accordingly.

FIG. **14** schematically shows the layout of the semiconductor device shown in FIG. **13**. The layout shown in FIG. **14** is identical to that shown in FIG. **11**, except that P-type active region **15** is removed from output circuit **1**, therefore corresponding parts are allotted with identical reference numerals or characters, and detailed description thereof will not be repeated.

In the layout shown in FIG. **14**, the drain contact-to-gate electrode distance Lpt of each of P-channel MOS transistors **11***a* and **11***b* of terminating circuit **10** is set shorter than the drain contact-to-gate electrode distance Lno of each of MOS transistors **4***a* and **4***b* of the output circuit, and preferably set to the minimum design size Lpt (min). Similarly, the drain contact-to-gate electrode distance Lnt of each of MOS transistors **15***a* and **15***b* of terminating circuit **10** is set shorter than the drain contact-to-gate electrode distance Lno of each of MOS transistors **4***a* and **4***b* in output circuit **1**, and preferably set to the minimum design size Lnt (min).

As shown explicitly in the layout in FIG. **14**, the layout area of active regions **30** and **32** in terminating circuit **10** can be reduced, and the layout area is also reduced in output circuit **1**, since only active region **19** is provided therein. Thus, an output circuit, driving the pad **5** in accordance with open-drain scheme at high speed with small occupying area, can be implemented. It should be noted that the ground voltage applied to terminating circuit **10** and the ground voltage applied to output circuit **1** may be applied from the same terminal, or may be from different terminals.

Third Modification

FIG. **15** shows a configuration of a third modification of the second embodiment of the present invention. The configuration shown in FIG. **15** is different from the semiconductor device shown in FIG. **13** in the following points. MOS transistors **11***a* and **11***b* for terminating at power supply voltage and resistance element **13** connecting to termination node **12** are provided in terminating circuit **10**. These MOS transistors **11***a* and **11***b* connect resistance element **13** to a power supply node in accordance with termination control signal ZTERM.

Output circuit **1** has identical configuration to that shown in FIG. **13**, and includes N-channel MOS transistors **4***a* and **4***b* for driving the pad **5** to ground voltage level via output node **3** in accordance with output control signal OTL.

In the configuration shown in FIG. **15** also, termination node **12** of terminating circuit **10** is electrically connected to pad **5** via output node **3** by interconnection line **50**. The distance L2 from termination node **12** to pad **5** and the distance L1 from output node **3** to pad **5** satisfy the relationship of L2>L2, and the surge is sufficiently mitigated by the parasitic low pass filter in interconnection line **50** before arrives at terminating circuit **10**. Therefore, the drain contact-to-gate electrode distance of each of MOS transistors **11***a* and **11***b* in terminating circuit **10** can be set to the minimum size permissible on designing (minimum design size).

FIG. **16** schematically shows the layout of the semiconductor device shown in FIG. **15**. The layout of the semiconductor device shown in FIG. **16** is different from that of the semiconductor device shown in FIG. **14** in the following points. Resistance element **14** and active region **32** are not provided in terminating circuit **10**, and instead, resistance element **13** and P-type active region **30** are provided. The other configuration is the same as that shown in FIG. **14**, thus corresponding parts are allotted with identical reference numerals or characters, and detailed description thereof will not be repeated.

In the layout shown in FIG. **16**, the drain contact-to-gate electrode distance Lpt of each of P-channel MOS transistors **11***a* and **11***b* is set shorter than the drain contact-to-gate electrode distance Lno of each of P-channel MOS transistors **4***a* and **4***b*, and set to the minimum design size Lpt (min).

As shown in FIG. **16**, terminating circuit **10** merely includes P-type active region **30** and resistance element **13**, and thus its layout area is reduced. Similarly, output circuit **1** merely includes N-type active region **19** and correspondingly, its layout area is reduced. The only restriction for interconnection line **50** is that both of termination node **12** and output node **3** must be connected to interconnection line **50** while satisfying the condition L2>L1.

FIG. **17** schematically shows overall configuration of a semiconductor circuit device according to the present invention. In FIG. **17**, a semiconductor circuit device **70** includes output circuit **1** for driving the pad **5** via output node **3** in accordance with output control signals ZOTH and OTL, and terminating circuit **10** for terminating the pad **5** at a prescribed voltage level via terminating node **12** in accordance with termination control signals ZTERM and TERM.

Output circuit **1** includes a pull-up transistor **2** for driving the output node **3** to power supply voltage level in accordance with output control signal ZOTH, and a pull-down transistor **4** for driving the output node **3** to ground voltage level in accordance with output control signal OTL. These pull-up transistor **2** and pull-down transistor **4** correspond to MOS transistors **2***a*, **2***b* and MOS transistors **4***a*, **4***b* as described in the first and second embodiments above, respectively. Terminating circuit **10** has the identical configuration to that shown in FIG. **9**.

Semiconductor circuit device **70** further includes a main control circuit **72** for controlling various specified operations in accordance with an external control signal, an internal circuit **74** performing a prescribed processing operation under the control of main control circuit **72** to generate output control signals ZOTH and OTL, and a termination control circuit **76** for generating termination control signals ZTERM and TERM under the control of main control circuit **72**.

When internal circuit **74** is a memory circuit, the output control signals ZOTH and OTL are generated through combination of an internal read data and an output control signal. When pad **5** is also used as an input pad for a signal input, then prescribed signal/data is applied to main control circuit **72** or internal circuit **74** via this pad **5**. When the output pad and the input pad are provided separately, then signals/data are applied to main control circuit **72** and internal circuit **74** via input pads that are not shown, respectively.

Termination control circuit **76** changes the state of termination control signals ZTERM and TERM in accordance with the usage condition of the bus to which semiconductor circuit device **70** is connected.

As output circuit **1** shown in FIG. **17**, open-drain type output circuit may be provided only with pull-down transistor **4**. Terminating circuit **10** may have any of the configurations shown in FIGS. **9** to **16**. To terminating circuit **10**, power supply voltage and/or ground voltage may be applied via the same terminal as output circuit **1**, or may be applied via different terminals.

As above, according to the second embodiment of the present invention, the terminating circuit and the output

circuit are connected via the common interconnection line, with the terminating circuit arranged further away from the pad as compared to the output circuit. Accordingly, a low pass filter is formed by the parasitic capacitance and the parasitic resistance of the interconnection line, which serves to mitigate the surge. Thus, the drain resistance of the transistors in terminating circuit can be reduced, and the drain contact-to-gate electrode distance can be reduced down to the minimum design size. Accordingly, the layout area of the signal/data output portion can be reduced.

The distance from gate electrode to drain contact corresponds to the distance from a portion of connecting drain node and an internal node together to a contacting portion (interface portion) of the drain region and the channel region. Usually in MOS transistor, a drain high electric field is generated in a portion just under the gate electrode of the drain region. By adjusting the distance to the interface between the drain and the channel through which signal charges propagate, the drain high electric field on occurrence of the surge can be relaxed. Accordingly, the distance between the drain contact and the gate electrode is the distance when seen in two-dimensional layout.

In the above configurations, output circuits are constructed with MOS transistors. Even when the output circuit is constructed with bipolar transistors, the same effect can be achieved by replacing the drain with a collector of a bipolar transistor and the gate with a base of the bipolar transistor.

As above, according to the present invention, the distance between one conduction node and the control electrode of the terminating transistor is set shorter than the distance between one conduction node and the control electrode of the first output transistor driving the output node in accordance with an internal signal. Accordingly, the layout area of terminating circuit can be reduced, and the semiconductor device containing the terminating circuit can be implemented without increasing the layout area.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a pad;

an output circuit including a P channel MOS transistor connected between said pad and a first voltage node, and an N channel MOS transistor connected between said pad and a second voltage node; and

a terminating circuit connected to said pad, and including a first terminating resistance element having one end connected to said pad, first and second P channel terminating unit transistors connected in parallel between another end of said first terminating resistance element and said first voltage node and sharing a first drain impurity region coupled to the other end of said first terminating resistance element, a second terminating resistance element having one end connected to said pad, and first and second N channel terminating unit transistors connected in parallel between another end of said second terminating resistance element and said second voltage node and sharing a second drain impurity region coupled to the other end of said second terminating resistance element.

2. The semiconductor device according to claim **1**, wherein

a distance between each gate of the first and second P channel terminating unit transistors and a drain contact connected to the shared first drain impurity region is shorter than a distance between a gate and a drain contact of said first P channel MOS transistor, and

a distance between each gate of the first and second N channel terminating unit transistors and a drain contact connected to the shared second drain impurity region is shorter than a distance between a gate and a drain contact of said first N channel MOS transistor.

3. The semiconductor device according to claim **1**, wherein

the P channel MOS transistor comprises first and second P channel MOS unit transistors connected in parallel with each other and sharing a third drain impurity region, and

the N channel MOS transistor comprises first and second N channel MOS unit transistors connected in parallel with each other and sharing a fourth drain impurity region.

4. The semiconductor device according to claim **3**, wherein

a distance between each gate of the first and second P channel terminating unit transistors and a drain contact connected to the shared first drain impurity region is shorter than a distance between each gate of the first and second P channel MOS unit transistors and a drain contact connected to the shared third drain impurity region, and

a distance between each gate of the first and second N channel terminating unit transistors and a drain contact connected to the shared second drain impurity region is shorter than a distance between each gate of the first and second N channel MOS unit transistors and a drain contact connected to the shared fourth drain impurity region.

5. A semiconductor device comprising:

a memory circuit;

a pad being used for outputting data read from said memory circuit;

a first N channel transistor pulling-down an output signal delivered to the pad in accordance with the read data, and having a first impurity region to be supplied with a first voltage, a second impurity region coupled to said pad via a first contact disposed thereon, and a first gate electrode disposed between the first impurity region and the second impurity region; and

a terminating circuit connected to the pad and being activated by a terminating operation activating signal and which includes a first terminating resistance element connected to said pad and a first P channel transistor having third and fourth impurity regions to be supplied with a second voltage, a fifth impurity region provided between the third impurity region and the fourth impurity region and coupled to said first terminating resistance element via a second contact disposed thereon, a second gate electrode disposed between the third impurity region and the fifth impurity region, and a third gate electrode disposed between the fourth impurity region and the fifth impurity region in parallel with said second gate electrode, said second gate electrode and said third gate electrode receiving the terminating operation activating signal, a first distance between said second contact and said second gate electrode being shorter than a second distance between said first contact and said first gate electrode.

6. The semiconductor device according to claim 5, wherein

the first distance and the second distance are the distance in the two dimensional layout.

7. The semiconductor device according to claim 5, wherein

a third distance between said second contact and said third gate electrode is shorter than the second distance.

8. The semiconductor device according to claim 5, further comprising a second P channel transistor pulling-up said output signal delivered to the pad in accordance with the read data, and having a first impurity region of the second P channel transistor to be supplied with a third voltage, a second impurity region of the second P channel transistor coupled to said pad via a third contact disposed thereon, and a first gate electrode of the second P channel transistor disposed between the first and the second impurity region of the second P channel transistor; and

wherein the terminating circuit includes a second terminating resistance element connected to said pad and a second N channel transistor having third and fourth impurity regions of the second N channel transistor to be supplied with a fourth voltage, a fifth impurity region of the second N channel transistor provided between the third impurity region and the fourth impurity region of the second N channel transistor and coupled to said second terminating resistance element via a fourth contact disposed thereon, a second gate electrode of the second N channel transistor disposed between the third impurity region and the fifth impurity region of the second N channel transistor, and a third gate electrode of the second N channel transistor disposed between the fourth impurity region and the fifth impurity region of the second N channel transistor in parallel with said second gate electrode of the second N channel transistor, said second gate electrode and said third gate electrode of the second N channel transistor receiving a terminating operation activating signal, a third distance between said fourth contact and said second gate electrode of said second N channel transistor being shorter than said second distance.

9. The semiconductor device according to claim 8, wherein

a fourth distance between said second contact and said third gate electrode of said first P channel transistor being shorter than a fifth distance between said third contact and said first gate electrode of said second P channel transistor.

10. The semiconductor device according to claim 9, further comprising:

a first power supply terminal supplying the first voltage and the fourth voltage; and

a second power supply terminal supplying the second voltage and the third voltage.

11. The semiconductor device according to claim 8, further comprising a first area and a second area which sandwich a virtual straight line which is located so as to pass on the pad,

wherein the first P channel transistor and the second P channel transistor are arranged in the first area, and the first N channel transistor and the second N channel transistor are arranged in the second area.

* * * * *

JS 44 (Rev. 11/04)

CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

I. (a) PLAINTIFFS

Renesas Technology Corp.

(b) County of Residence of First Listed Plaintiff Japan
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorney's (Firm Name, Address, and Telephone Number) John M. Seaman
Bouchard Margules & Friedlander (302) 573-3500
222 Delaware Avenue, Ste 1400, Wilmington, DE 19801

DEFENDANTS

Samsung Electronics Co. Ltd. and
Samsung Electronics American, Inc.

County of Residence of First Listed Defendant Korea
(IN U.S. PLAINTIFF CASES ONLY)

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE LAND INVOLVED.

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff
- XX 3 Federal Question (U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In This State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT (Place an "X" in One Box Only)

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

TORTS

PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury - Med. Malpractice
- ☐ 365 Personal Injury - Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 444 Welfare
- ☐ 445 Amer. w/Disabilities - Employment
- ☐ 446 Amer. w/Disabilities - Other
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence

Habeas Corpus:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

FORFEITURE/PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R.R. & Truck
- ☐ 650 Airline Regs.
- ☐ 660 Occupational Safety/Health
- ☐ 690 Other

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt. Relations
- ☐ 730 Labor/Mgmt.Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl. Ret. Inc. Security Act

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- ☐ 820 Copyrights
- XX 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS—Third Party 26 USC 7609

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 890 Other Statutory Actions
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Information Act
- ☐ 900Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes

V. ORIGIN (Place an "X" in One Box Only)

XX 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing (**Do not cite jurisdictional statutes unless diversity**): 35U.S.C. Sec.101

Brief description of cause: Patent Infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER F.R.C.P. 23 DEMAND $

CHECK YES only if demanded in complaint:
JURY DEMAND: XX Yes ☐ No

VIII. RELATED CASE(S) IF ANY (See instructions): JUDGE Other patent infringement cases filed by plaintiff this same day. DOCKET NUMBER

DATE January 26, 2007

SIGNATURE OF ATTORNEY OF RECORD John M Seaman

FOR OFFICE USE ONLY

RECEIPT # AMOUNT APPLYING IFP JUDGE MAG. JUDGE

JS 44 Reverse (Rev. 11/04)

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

I. (a) Plaintiffs-Defendants. Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

(b) County of Residence. For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)

(c) Attorneys. Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".

II. Jurisdiction. The basis of jurisdiction is set forth under Rule 8(a), F.R.C.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.

United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here.

United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.

Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.

Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; federal question actions take precedence over diversity cases.)

III. Residence (citizenship) of Principal Parties. This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

IV. Nature of Suit. Place an "X" in the appropriate box. If the nature of suit cannot be determined, be sure the cause of action, in Section VI below, is sufficient to enable the deputy clerk or the statistical clerks in the Administrative Office to determine the nature of suit. If the cause fits more than one nature of suit, select the most definitive.

V. Origin. Place an "X" in one of the seven boxes.

Original Proceedings. (1) Cases which originate in the United States district courts.

Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441. When the petition for removal is granted, check this box.

Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.

Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.

Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.

Multidistrict Litigation. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407. When this box is checked, do not check (5) above.

Appeal to District Judge from Magistrate Judgment. (7) Check this box for an appeal from a magistrate judge's decision.

VI. Cause of Action. Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553
Brief Description: Unauthorized reception of cable service

VII. Requested in Complaint. Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.

Demand. In this space enter the dollar amount (in thousands of dollars) being demanded or indicate other demand such as a preliminary injunction.

Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

VIII. Related Cases. This section of the JS 44 is used to reference related pending cases if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.

AO FORM 85 RECEIPT (REV. 9/04)

United States District Court for the District of Delaware

Civil Action No. CA 07-53

ACKNOWLEDGMENT OF RECEIPT FOR AO FORM 85

NOTICE OF AVAILABILITY OF A UNITED STATES MAGISTRATE JUDGE TO EXERCISE JURISDICTION

I HEREBY ACKNOWLEDGE RECEIPT OF 3 COPIES OF AO FORM 85.

1/26/07
(Date forms issued)

(Signature of Party or their Representative)

KEVIN LALLY
(Printed name of Party or their Representative)

Note: Completed receipt will be filed in the Civil Action